

AI Datacenter: Power System Architecture

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1. Introduction

This Techbook explores the technologies enabling the next generation of AI datacenters, where unprecedented computing demand is driving a fundamental transformation in power delivery, energy efficiency, and system architecture. As AI training and inference workloads continue to expand, datacenters are scaling from tens of kilowatts per rack to hundreds of kilowatts, with future deployments expected to approach megawatt-class rack power levels. These trends are accelerating the adoption of high-voltage Direct Current (DC) distribution, solid-state transformers, advanced power conversion topologies, battery energy storage integration, and increasingly sophisticated system monitoring and control infrastructures.

Nothing speaks more about the importance and growth pace of datacenters than their electricity demands. It is estimated (IEA, Energy and AI, April 2025 & McKinsey, Datacenter demand model, 2025) that a compound annual growth of 14% globally doubles consumption from 440 TWh in 2024 to 968 TWH in 2030. The United States and China dominate the consumption share with 75% of the total demand, with hyperscaler datacenter projects often exceeding the 1 GW consumption. Training and interference of generative AI models require enormous amounts of computing power. Global investments in data centers are expected to amount to $1.1 trillion USD by 2029. Companies like Meta, Amazon, Alphabet or Apple aim to invest over $100 billion each in datacenters in the coming years. Individual Rack powers are also seen as exponentially increasing. While it was put at 1 kW in the 2000's by 2020 the expected consumption rose to 20 kW with newer designs such as NVIDIA GB200 NVL2 going up to 200 kW and future projections often citing the 1 MW power level in sight.

To address these challenges, this Techbook examines the key power and signal integrity problems encountered throughout modern AI datacenter architectures, from facility-level power conversion systems to server motherboard communications. It highlights the roles of silicon carbide (SiC) and gallium nitride (GaN) semiconductor technologies in achieving higher efficiency, power density, and reliability, while also covering critical functions such as hot-swap protection and digital isolation. Through practical design examples and application-focused solutions, the book provides engineers with insights into the technologies required to build resilient, efficient, and scalable AI datacenter platforms.

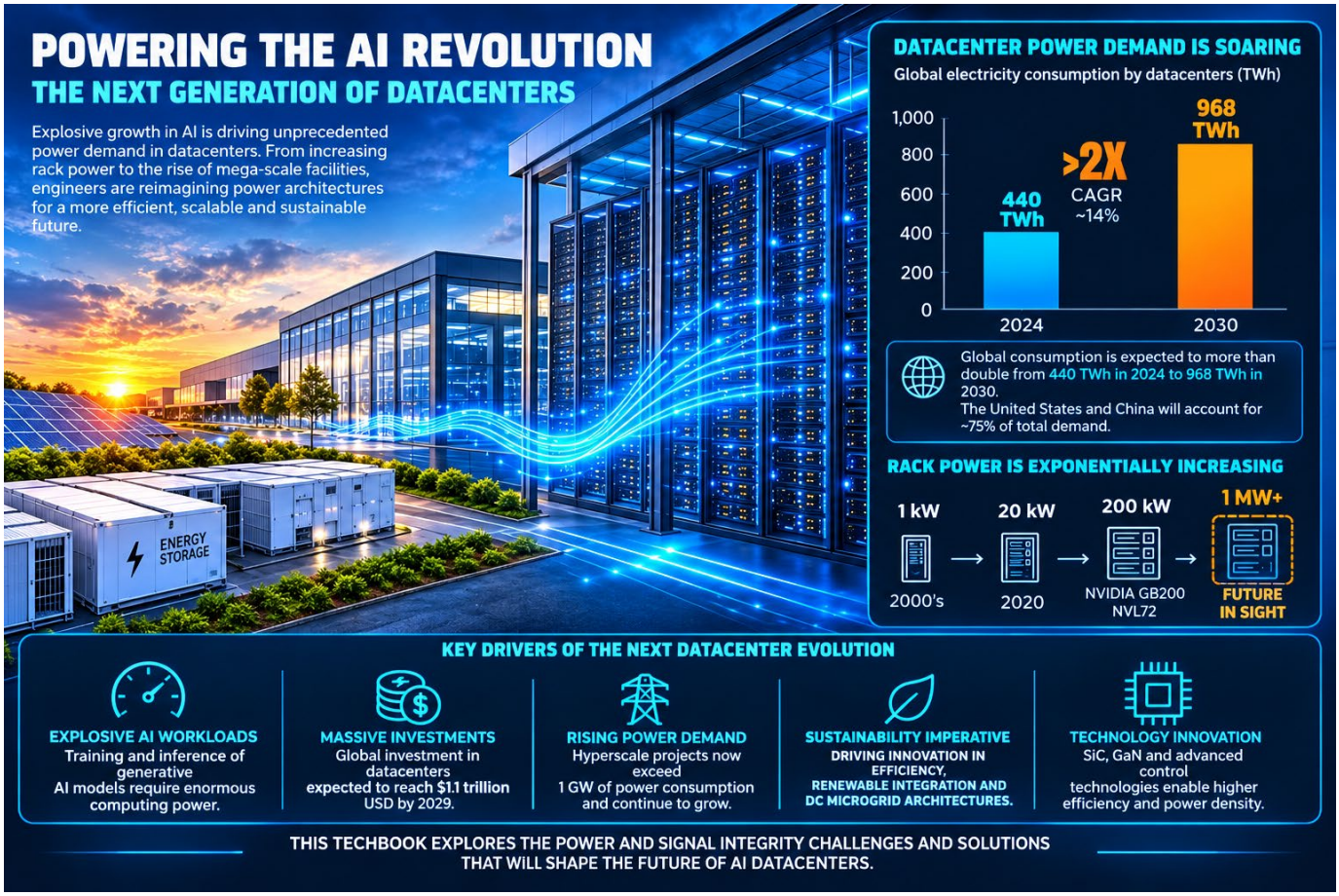


Fig. 1 Datacenter power demand growth

2. Datacenter trends

Datacenters can in general be of varied sizes:

- Edge & Micro Data Centres (~ 1 kW)- Often a single room or cabinet, built locally to process data near the end-user (e.g., at a 5G cell tower base).
- Enterprise (Private) Data Centres (~ 10 kW)- custom-built within an organisation's headquarters or dedicated company site.
- Managed Services Data Centres (~ 500 kW) - Medium-to-large commercial buildings operated by third parties for outsourced IT setups.
- Colocation Data Centres (~ 5 MW) - Large multi-tenant warehouses that hold thousands of server racks for multiple companies.
- Cloud Data Centres (~100 MW) - Massive industrial compounds designed for regional digital traffic.
- Hyperscale Data Centres (~500 MW) - Global mega-facilities featuring a minimum of 5,000 tightly packed, highly automated server racks.
- Next gen AI hyperscale (~1 GW) - Designed for large AI training and inference clusters

To address the most generic technical challenges this booklet will deal with hyperscalers as they are the largest, contain all the elements of the smaller datacenters from the power and signal processing perspective and contain the latest technological advances.

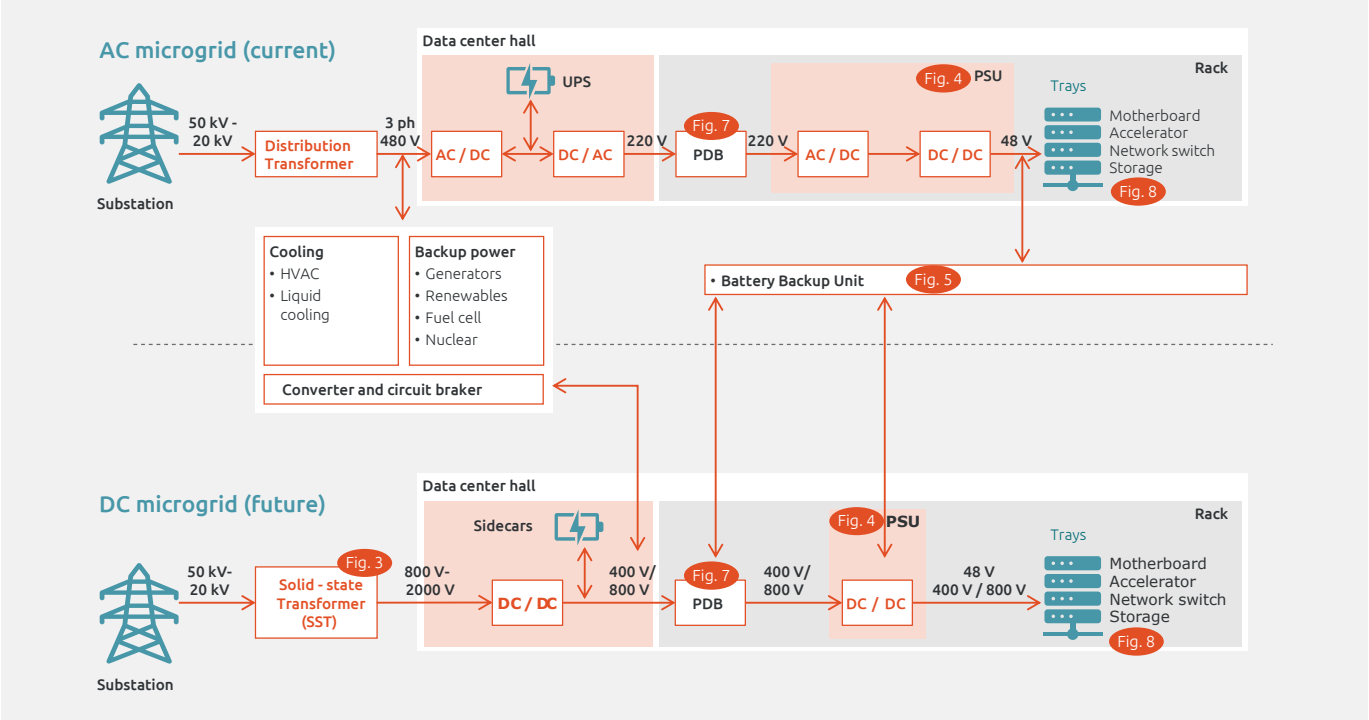


Fig. 2 Vehicle control unit architecture development

Fig. 2 shows two different approaches to the datacenter power delivery architectures. There is an ongoing shift from Alternating Current (AC) to DC microgrids that represents a massive structural redesign. It is driven by extreme density of modern AI clusters, the tendency towards 800V DC direct power supply to the IT trays and the need to integrate renewable energy to satisfy the large power demand.

In a standard AC-distributed microgrid, power goes through a highly inefficient "conversion roller coaster" before it ever reaches a computer chip. High-voltage AC from the utility grid is stepped down to medium-voltage ac, then converted to DC to charge the Uninterruptible Power Supply (UPS) batteries. The UPS converts that DC back into AC for facility distribution. Finally, individual Power Supply Units (PSUs) inside each server rack convert that AC back to DC to power the processors. Every single one of these conversion stages introduces heat and wastes useful energy.

A DC microgrid eliminates the middle steps. Grid or onsite power is converted to Direct Current exactly once at the facility perimeter (using a Solid-State Transformer (SST) or massive rectifiers). From there, power travels natively as DC all the way to the chip.

Some of the current trends in furthering power delivery capabilities include:

- High-voltage step-up (Moving to 800V and 1500V DC) - Higher voltage drops current demands, which slashes resistive energy losses and lets data centres use less copper cabling, which also makes cable installation easier.
- Native integration of distributed energy resources (DERs) - Modern data centre microgrids increasingly generate their own power onsite via solar PV arrays, fuel cells, and Battery Energy Storage Systems (BESS). All of these technologies naturally generate or store power as DC enabling easy coupling to the DC microgrid infrastructure.
- Elimination of the "Power Shelf" via Rack Sidecars - Massive, centralized industrial rectifiers sit in adjacent rooms or dedicated power racks. This frees up space in each compute rack for extra processing hardware.
- The death of synchronization problems - In an AC microgrid, blending power from the utility grid, localized backup generators, and solar fields requires sophisticated, complex control loops to synchronize voltage phase and frequency. Because DC has no phase or frequency, synchronization and reactive power losses are eliminated, drastically simplifying microgrid stability control.

After the introduction of the basic functional block diagrams of the main power and signal conversion systems within a datacenter, this booklet will be organised in two sections. First, high power conversion will be addressed with solid state transformers and large scale rectifiers topologies, along with high power DC/DC converters needed for green energy and BESS integration. Next, low power conversion will be described including local DC/DC conversion, hot swap functionality and low voltage power distribution.

3. Block diagrams

The individual block diagrams of some of the components of interest are shown in Fig. 3 to Fig. 8. Starting with block diagrams focusing on power stages of converters, they are represented as converter steps that change the qualities of the electric energy transferred, with highlighted components from Nexperia that can be designed into them.

As electrical power enters the datacenter premises, whether it is supplied by the power grid, renewable sources or local (nuclear) power plants, invariably, large power converters meet it and convert to a format more readily accessible to the server racks and other auxiliary equipment. Historically the greeting converters were high and medium voltage line transformers. However, lately SSTs (Fig. 3) are being used. By one approach SSTs can be any converter that is comprised of modules containing high frequency power transformers. For datacenters specifically, an ISOP – Input Series Output Parallel connection of isolated ac to DC converters are used. This allows the input side of the converter to be rated to lower voltage than the actual grid voltage it handles, as the input voltage is divided across multiple converter module inputs. Conversely, because of the parallel output configuration the currents add up from the individual modules, while each module provides the same output voltage. At the input of the SST module an AC to DC or Power Factor Correction converter changes the input high voltage AC to DC power in each module. The power is then converted to high frequency AC to be passed through a small high frequency transformer and rectified at its output to the required 400 V or 800 V DC distribution voltage. Each individual module needs its own control and communication electronics and the whole system also needs a supervisory and synchronising controller, surrounded by signal conditioning and communication circuitry.

For a successful wide deployment of SSTs a number of technical challenges need attention. Complexity stems from the individual converters: electrical and thermal management, signal level electronics, auxiliary power supplies and communication interfaces with adequate isolation. Further, the joint management and redundancy requirements pose further challenges. Achieving benchmarks in power density are challenging as well: the high frequency transformer size reduction due to frequency is limited by high voltage safety isolation needs. The high voltage isolation also necessitates larger creepage and clearance distances along with adequate isolation materials and distances between two modules or a module and the enclosure. Therefore power densities of SSTs do not achieve the merits of lower voltage See SST article.

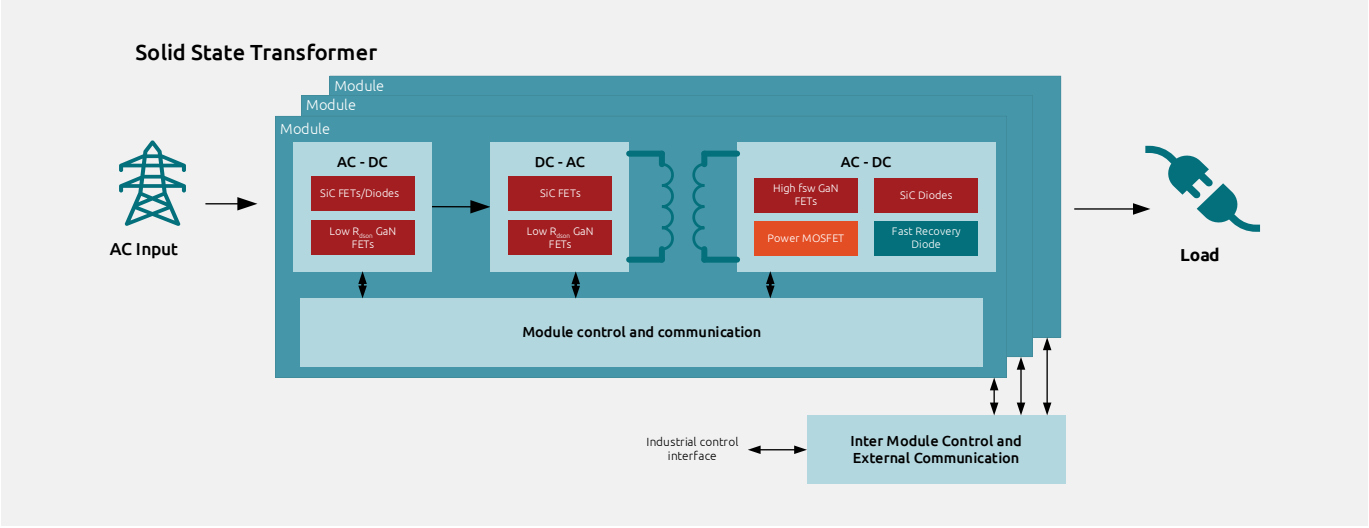


Fig. 3 Solid State Transformer block diagram

In case a traditional power transformer is used to lower the input voltage to the datacenter, individual power supply units (Fig. 4) are used to convert the now low voltage AC power to DC power at rates needed by individual servers, server rooms or halls depending on the power requirement and power system architecture of the datacenter. The power supply units are comprised of an input PFC controller and an output DC/DC controller that provides the DC distribution voltage. The power conversion is once again supervised by a control and communication circuit that reads the needed currents and voltages of the system, provides gating signals to the power electronics and at the same time communicates the system state and performance and receives control instructions from a high-level control panel.

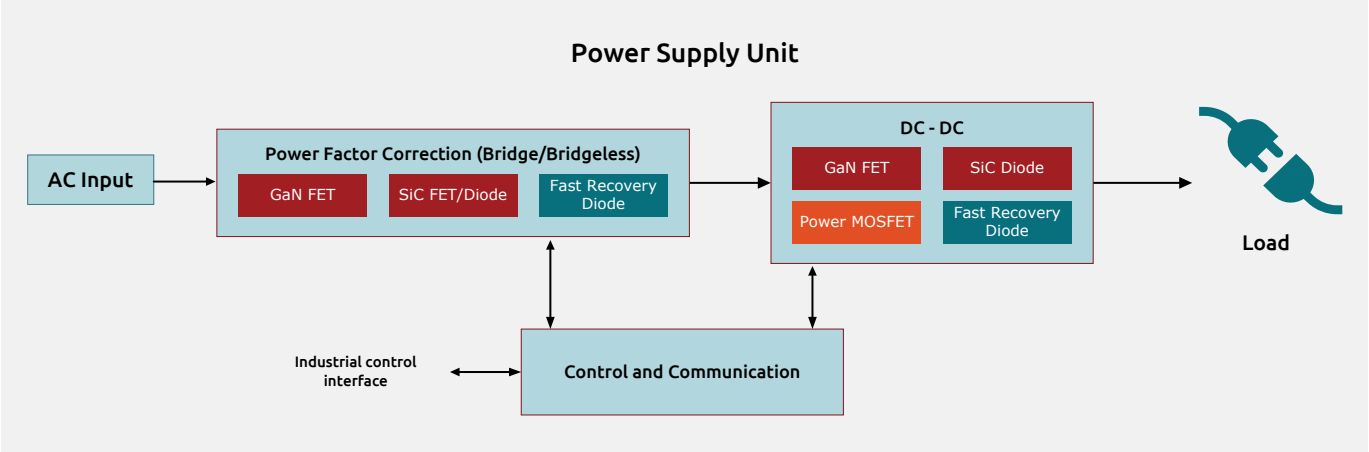


Fig. 4 Power Supply Unit block diagram

A Battery Backup Unit (Fig. 5) provides the short-term energy storage required to maintain uninterrupted operation of AI datacenter infrastructure during utility disturbances, power-conversion faults, or transitions between primary and backup energy sources. In emerging DC datacenter architectures, the BBU is increasingly integrated directly into the DC distribution network, eliminating unnecessary AC/DC conversion stages and improving overall system efficiency. The BBU typically consists of a high-voltage battery stack, battery management system (BMS), bidirectional DC/DC power converters, protection circuitry, and supervisory control electronics. During normal operation, the converter regulates battery charging while continuously monitoring cell voltage, temperature, state-of-charge, and state-of-health parameters. The control and communication subsystem exchanges telemetry with higher-level datacenter energy-management controllers to optimize battery utilization, maintenance scheduling, and system reliability.

When a power interruption or load transient occurs, the bidirectional DC/DC converter rapidly reverses power flow, allowing the battery system to supply energy to the DC bus with minimal disturbance to critical computing loads. As AI server racks continue to increase in power density, BBUs must deliver extremely high transient currents while maintaining tight voltage regulation and high conversion efficiency. This creates demanding requirements for power semiconductors, gate drivers, sensing circuits, isolation devices, and hot-swap protection components. Wide-bandgap technologies such as GaN enable higher switching frequencies, reduced magnetic component size, and improved power density in these battery-interface converters, making them particularly attractive for modern AI datacenter backup-power architectures.

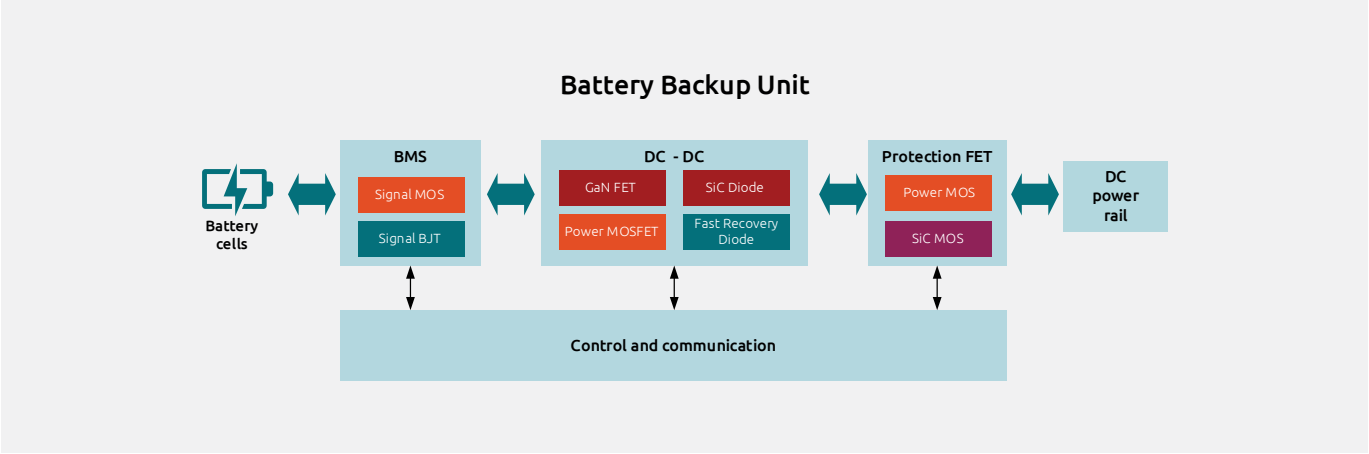


Fig. 5 Battery Backup Unit block diagram

The Control and Communication block (Fig. 6) forms the intelligence layer of modern datacenter power converters, providing real-time monitoring, regulation, protection, and system-level coordination. It continuously measures key operating parameters such as input and output voltages, currents, temperatures, battery status, and fault conditions, processes this information using digital controllers or microcontrollers, and generates the gate-drive commands required for efficient converter operation. At the same time, it communicates with supervisory datacenter management systems through interfaces such as I²C, PMBus, SMBus, CAN, or Ethernet, enabling telemetry reporting, remote configuration, predictive maintenance, redundancy management, and coordinated control of multiple power-conversion modules. Because these functions frequently span different voltage domains, the subsystem also incorporates isolation, signal conditioning, timing, and protection circuitry to ensure reliable operation in electrically noisy environments created by fast-switching SiC and GaN power semiconductors. As a result, the Control and Communication block acts as the central nervous system of the power architecture, ensuring safe, efficient, and coordinated operation of SSTs, PSUs, BBUs, and other power-conversion stages throughout the AI datacenter. The technical challenges associated with signal and data conditionaing are addressed in a separate techbook (AI Datacenters – Signal conditioning), that you can find on the Nexperia website.

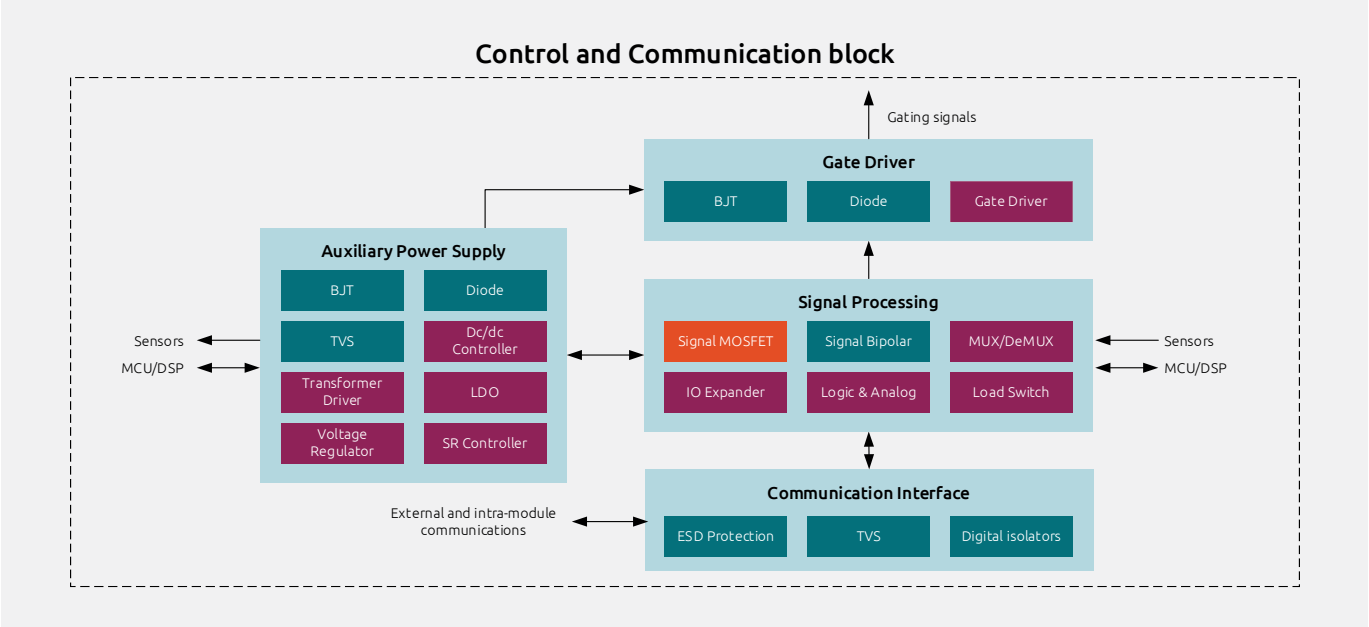


Fig. 6 Control and Communication block diagram

The power delivery board is an extension of the power supply unit. It converts the incoming 48V, or possibly 400 to 800V in the future, to 12V. It takes over some of the power delivery functions of the server motherboards as it delivers to the Motherboards, Network Switch, PCIe cards and fans the necessary 12V. The Power Input Protection block consists of high power (5kW) TVS diodes and a Hot swap controllers supported by up to 30 100V hot-swap MOSFETs often in parallel configuration. The Power Management section consists of buck converters and controllers of different power ratings that convert the incoming 48V to 12V. 80V LDOs can also be used as point of load converters.

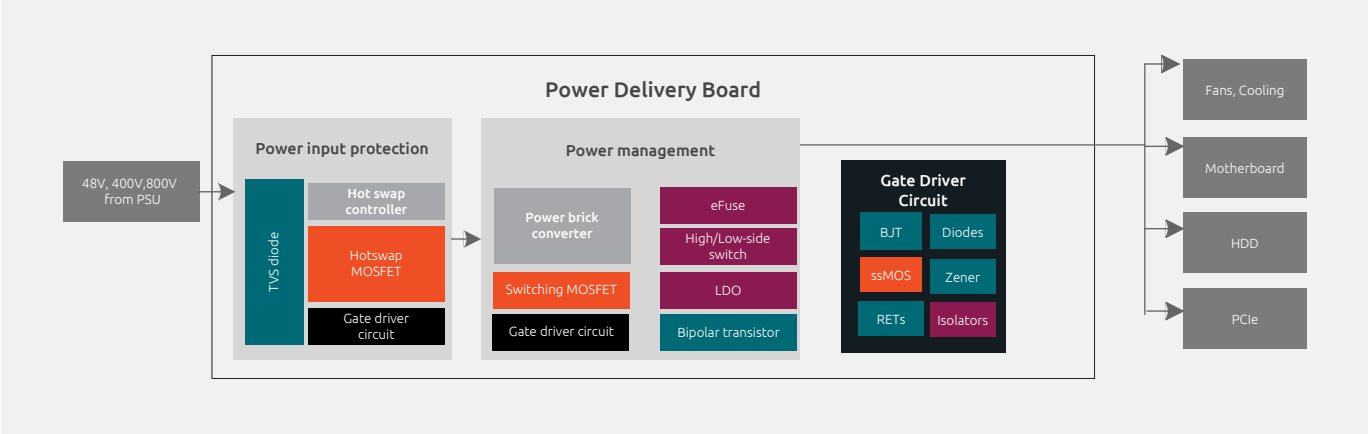


Fig. 7 Power Delivery Board block diagram

The motherboard hosts, powers and interconnects various parts of the computation side of the server. The parts connecting to the motherboard are listed on the right of the diagram in Fig. 8. Accelerators can have their own motherboard/tray or connect to the server motherboard via PCIe. Supply to the motherboard can be 12V, 48V or 54V. In the future this might extend to higher voltages of 400V and 800V for servers with extra-high power demand. The power input protection block contains TVS diodes for power surges. It also contains Ideal diodes, eFuses and Hot-swap controllers for reverse battery protection and inrush current protection. They protect the supply from the server as much as the server from the supply. Their isolator switches might be internal or external. The Power Management consist of multiple converters mostly with integrated switches to create the right voltage to each of the connected parts as well as the processors on the board itself. The Communication interface requires mostly fast, low voltage ESD diodes. Buffers and transceivers are often required for signal enhancements for longer communication lines and board to board communication. The technical challenges associated with signal and data conditionaing are addressed in a separate techbook (AI Datacenters – Signal conditioning), that you can find on the Nexperia website.

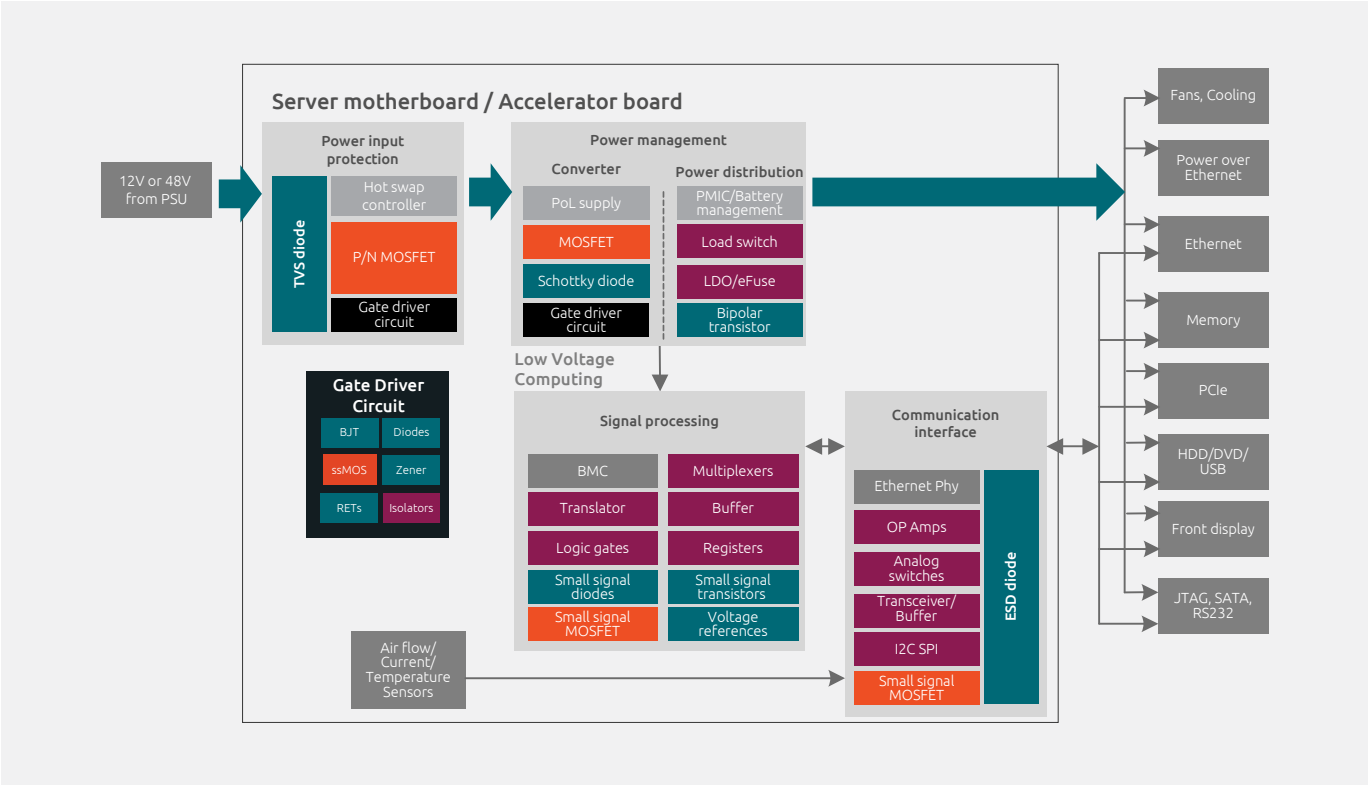


Fig. 8 Server Motherboard Block diagram

4. Design challenges in SST and PSU

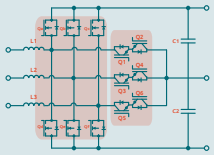
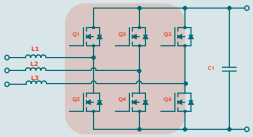
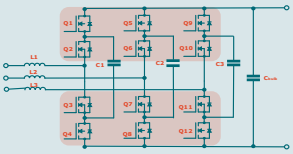
	 T-type NPC	 Active Front End PFC	 3L Flying capacitor PFC
Power Flow	Bidirectional	Bidirectional	Bidirectional
Device Stress	› ½ DC bus voltage for Q1-6 › Full DC bus voltage for Qa-f › Low RMS current per switch	› Full DC bus voltage › High RMS current per switch	› ½ DC bus voltage › High RMS current per switch
Device Choice	› Q_{a-f} **750/1200V** SiC MOS for bidirectional T-type PFC **NSF020750T1B0** QDPAK **NSF040750T1B0** QDPAK **NSF017120L4A0** TO247 4L **NSF030120T1A0** TO247 4L › Q_{a-f} can be replaced by **SiC Schottky diodes**, unidirectional power flow, low V_F, 20-40A 2x **PSC20120L** › Q_{1-6} **650V GaN**, 150–300 kHz switching frequency in TOLL/TOLT bidirectional 30 - 110 mΩ	› Q_{1-6} **1200 V SiC** in TO247 4L and QDPAK– robust avalanche capability, better short circuit with stand time **NSF017120T1A0 QDPAK** **NSF030120T1A0 QDPAK** **NSF017120L4A0 TO247 4L**	› Q_{1-12} **650V GaN**, 150–300 kHz switching frequency in GeN2 TOLL/TOLT 35 and 70mΩ **GANC035-650TBH, -UTH** **GANC050-650TBH, -UTH** **GANC070-650TBH, -UTH** › **750V SiC** 50mΩ TO247 **4L** **NSF020750T1B0 QDPAK** **NSF040750T1B0 QDPAK** **NSF020750L4B0 TO247 4L** **NSF040750L4B0 TO247 4L**
Advantages	› Lower dv / dt at phase nods › Smaller EMI filter › Higher power density	› Lower device count › Higher fault tolerance	› Inductors and caps see double switching frequency
Challenges	For Q_{1-6} : › Gate drive isolation › Layout › dv / dt induced false turn on For Q_{a-f} › Higher device stress › More demanding thermal design	› Higher device stress › More demanding thermal design › Lower switching frequency › Larger magnetics › Gate drive isolation and power › EMC	› Flying capacitor needs pre-charging › Increased number of gate drivers › Increased number of switches
Control Difficulty	Moderate | Phase current control, capacitor voltage balancing, no grid synch	High | vector control, PLL, power factor control	Flying cap balancing increases control algorithm complexity

Table 1 Common high power conversion PFC rectifier topologies

Table 1 compares three common high-power three phase PFC topologies used in large datacenters and highlights the relationship between topology, semiconductor device requirements, efficiency, and implementation complexity.

The T-type NPC is a bidirectional topology in which the active switches Q_{1-6} experience approximately half of the DC bus voltage and relatively low RMS current. These characteristics make 650 V GaN devices suitable for high-frequency operation. Q_{a-f} experience the full DC bus voltage and SiC MOSFET are better suited here. Q_{a-f} can be replaced by SiC diodes which turns the T-type NPC into Vienna rectifier with unidirectional power flow. More information about Nexperia SiC diodes can be found in our blogs (Why all SiC Schottky diodes are not made equal , 8 Reasons Why Silicon Carbide Diodes Outperform their Silicon Peers), brochures (From SiC to thin SiC diodes) and videos (Switching Performance of Silicon Carbide vs. Silicon Diodes, MPS Silicon Carbide Power Diodes Explained)

The Active Front End (AFE) supports bidirectional power flow as well. Its switches must withstand the full DC bus voltage and higher RMS current. Therefore, higher-voltage devices such as 1200 V SiC MOSFETs are preferred. The AFE benefits from a lower device count and good fault tolerance, although this comes at the cost of higher semiconductor stress, increased thermal requirements, and more demanding control.

The three-level flying-capacitor PFC also provides bidirectional operation while limiting the voltage stress of each switch to approximately half of the DC bus voltage. The output current ripple is also at double the semiconductor switching frequency. This enables the use of 650 V GaN devices and can provide very high efficiency and power density. However, the topology requires a larger number of semiconductor switches and gate drivers. In addition, the flying capacitors must be pre-charged, and their voltages actively balanced during operation, increasing both hardware and control complexity. Consequently, the flying-capacitor topology is attractive for future high-power-density converters, but its increased component count, cost, and control requirements currently make its implementation more challenging.

4.1 Ensuring safe and reliable control of the switching devices

Modern AI datacenter power systems rely on multiple high-performance switching stages including PFC converters, LLC resonant converters, intermediate bus converters, battery backup units and voltage regulator modules. These stages increasingly employ SiC and GaN power devices operating at very high switching speeds to maximize efficiency and power density. However, fast switching transients, high bus voltages, ground potential differences and common-mode noise make it increasingly difficult to deliver accurate gate-drive signals while maintaining safe isolation between the control and power domains. A loss of signal integrity or an isolation failure can result in mistimed switching events, increased losses, shoot-through currents or catastrophic power-stage failure. Ensuring reliable communication between the digital controller and the switching devices is therefore a critical design challenge in next-generation datacenter power architectures.

Nexperia addresses this challenge with isolation and gate-driver solutions. An application example in datacenters can be seen in Fig. 9. The NXF650x transformer-driver family generates compact isolated auxiliary bias supplies for digital isolators, gate drivers, and control circuitry, while the NXI772x digital isolator enables reliable communication across the isolation barrier. On the power-stage side, the NGD31251 dual-channel low-side gate driver supports synchronous rectification and interleaved converter topologies with 5 A source/sink capability, while the NGD4300 half-bridge driver enables high-side and low-side MOSFET control up to 120 V with excellent timing matching and switching robustness. Together, these devices form a scalable isolated gate-drive architecture that helps ensure safe switching, improved efficiency, and robust operation throughout the datacenter power-delivery chain.

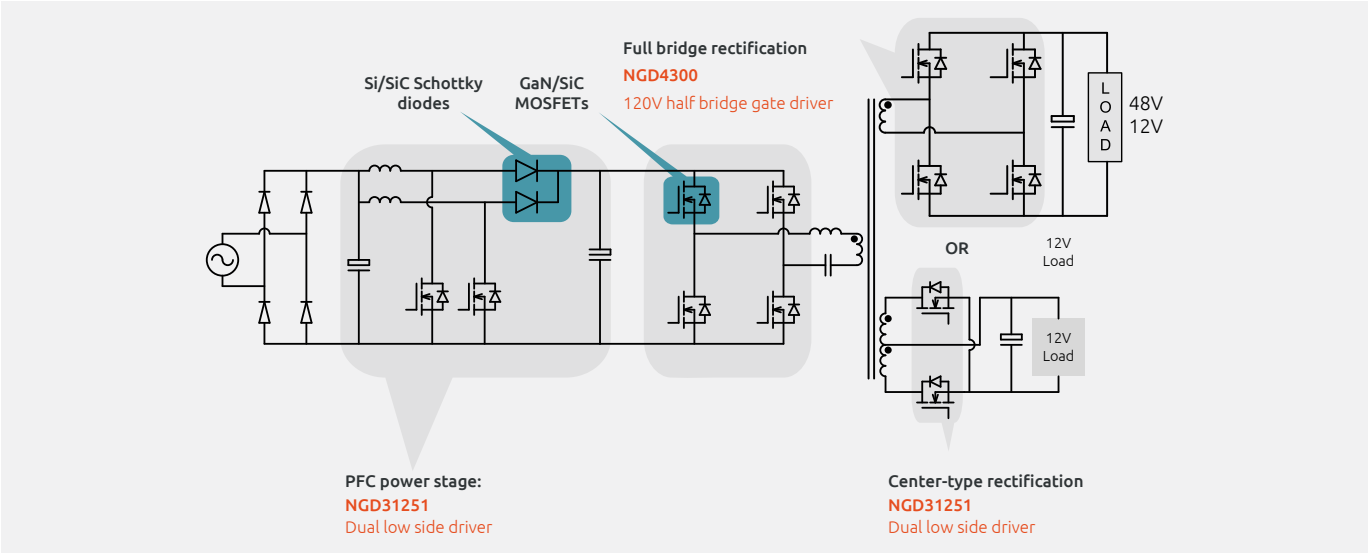
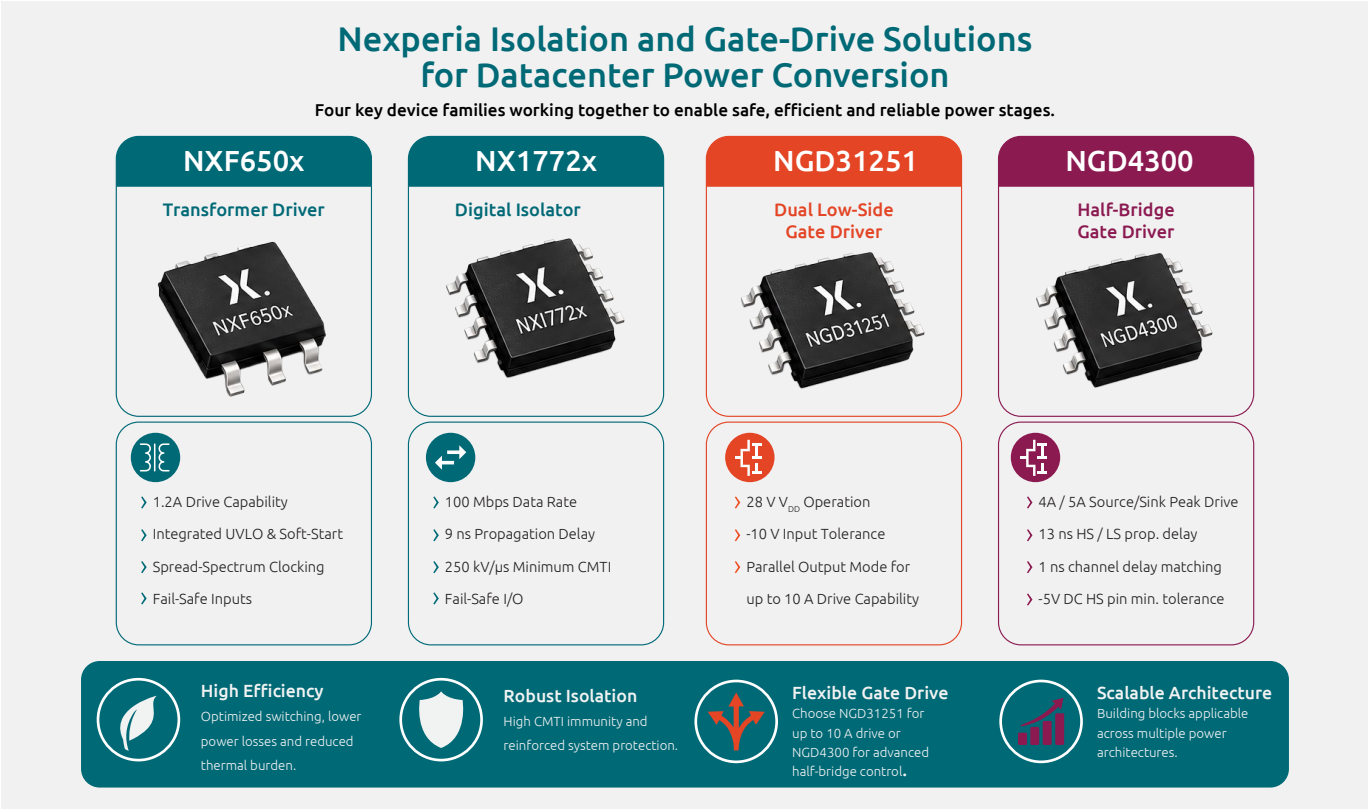


Fig. 9 Example power supply unit topology



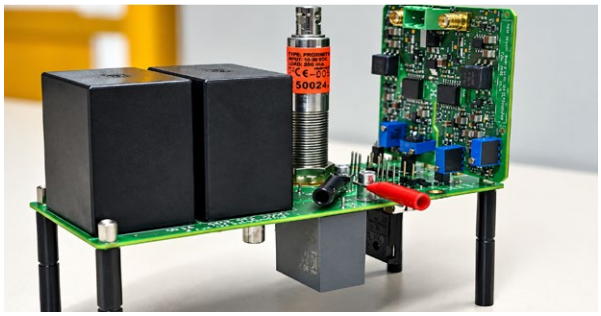
4.2 Selecting SiC MOSFET switches for best efficiency and EMC performance for PFC topologies.

The basis of all three topologies discussed in Table 1 is the half bridge. Therefore, half bridge reference designs can be used to evaluate switch performance and compare semiconductor devices. Nexperia provides a range of evaluation boards (EVBs) that are either available online or on demand. These boards support different stages of device evaluation, from initial package and gate-driver comparison to detailed characterization of selected devices.

The evaluation process can begin with NexFLEX, a modular platform that allows different semiconductor packages and gate-driver configurations to be tested using the same basic setup. This makes it particularly useful for comparing device technologies and package options under similar operating conditions.

Once a suitable device and package have been selected, more specialized evaluation boards can be used for further and more accurate characterization including Double Pulse Testing (DPT), Short Circuit Testing (SCT) and continuous operation. These platforms are designed to reproduce representative operating conditions and are also used for measurements associated with Nexperia datasheet characterization.

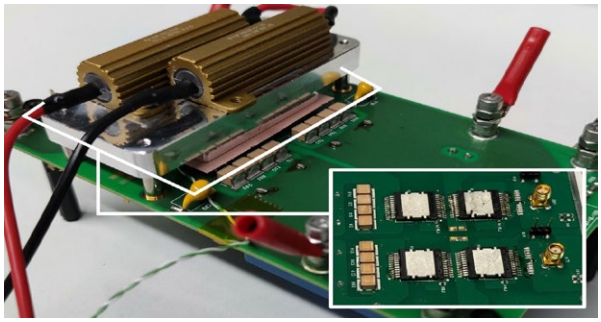
Depending on the platform, the boards can additionally support hard- and soft-switching, as well as operation in DC/DC and DC/AC configurations.



NexFLEX — Modular Platform

Availability: On demand

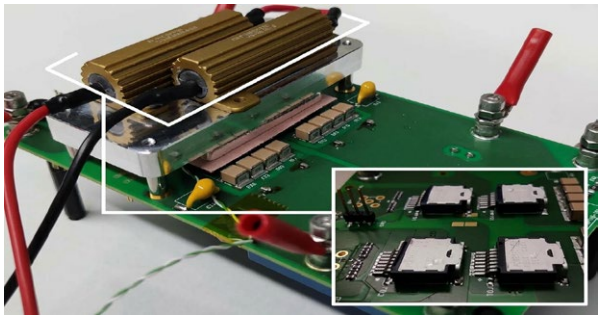
- Modular platform supporting multiple Nexperia packages
- Enables package-to-package and gate-driver comparisons
- Exchangeable gate-driver board
- Supported packages include X.PAK, QDPAK, D2PAK-7 and TO247-4
- Supports DPT, SCT and continuous operation



Top-Side Cooling QDPAK Platform

Availability: On demand

- Specialized platform for evaluating top-side-cooled packages
- Exchangeable gate-driver board
- Supports DPT and continuous operation
- Configurable as a single half-bridge, two half-bridges or a full bridge
- Supports hard- and soft-switching
- Suitable for DC/DC and DC/AC operation



Top-Side Cooling X.PAK Platform

Availability: Online

- Specialized platform for evaluation of top-side-cooled X.PAK devices
- Exchangeable gate-driver board
- Supports DPT and continuous operation
- Configurable as a single half-bridge, two half-bridges or a full bridge
- Supports hard- and soft-switching
- Suitable for DC/DC and DC/AC operation



D2PAK-7 Evaluation Board

Availability: Online

- Enhanced PCB design with minimized commutation-loop inductance
- Adjustable switching speed and gate voltage
- Current measurement using an SMD shunt
- DC-link capacitor and power layout designed for applications up to 1200 V
- Supports dynamic device characterization and in-application testing. User documentation available online

When selecting a semiconductor FET switch there are a few slightly hidden but very important characteristics to pay attention to in order to extract best performance. Beyond the basic current, voltage and cooling capabilities of the device, here are some of the key MOS/GaN/SiC FET requirements that are demonstrated in greater detail on the example of Nexperia SiC MOSFETs (Discover 4 Advantages of Nexperia's SiC MOSFETs, AN90048 Understanding of critical SiC parameters for efficient and stable designs, AN90067 X.PAK SiC MOSFETs: A Technical Guide, AN90074 Comprehensive Benchmarking of 1200V SiC MOSFETs in D2PAK7):

- › Excellent $R_{DS(on)}$ temperature stability → Very low conduction & switching losses
- › Tight threshold voltage specification → Easy parallel operation
- › Superior gate charge ratio → Safe & stable switching performance
- › Robust, low forward voltage body diode → Relaxed dead time requirements
- › Reverse recovery charge and type → Lower switching losses and better EMC performance.

A low $R_{DS(on)}$ at 25 °C is an important performance indicator for a MOSFET, but its behaviour at elevated junction temperatures is equally important. As shown in Fig. 10, the competitor devices exhibit an $R_{DS(on)}$ increase of approximately doubling the value on 25 °C at 175 °C, whereas the Nexperia SiC MOSFET shows a significantly smaller increase. The performance from Fig. 10 is recorded on NSF040120L4A0 but other devices also have similar performance.

This lower $R_{DS(on)}$ temperature drift allows the device to maintain better conduction performance at elevated temperatures and can therefore reduce conduction losses in high-power applications.

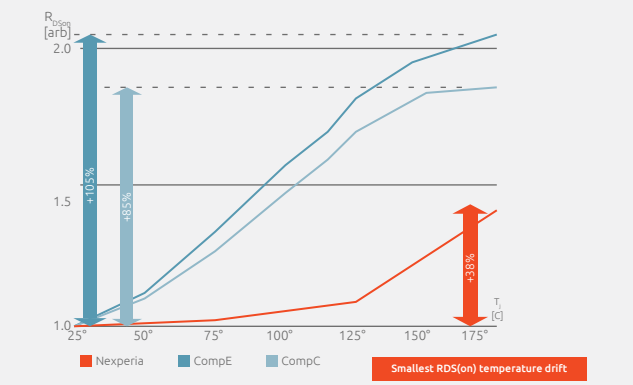


Fig. 10 Normalized $R_{DS(on)}$ temperature drift of Nexperia and competitor SiC MOSFETs

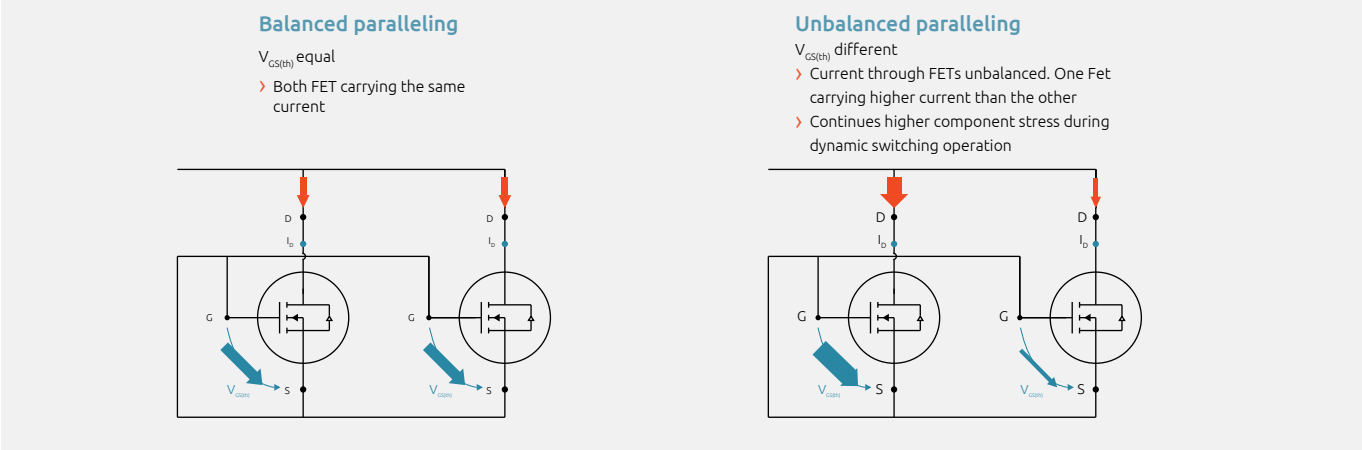


Fig. 11 Balanced and unbalanced current sharing in paralleled MOSFETs caused by $V_{GS(th)}$ variation

The gate-source threshold voltage, $V_{GS(th)}$, is a key MOSFET parameter because it determines the gate voltage at which the device begins to conduct. In high-power applications, particularly when several MOSFETs are operated in parallel, it is not only the absolute threshold voltage that matters, but also how closely this value is matched from device to device, as illustrated in Fig. 11.

Ideally, paralleled MOSFETs should turn on and off at approximately the same gate-source voltage so that the current is shared evenly between the devices. If the threshold voltages are poorly matched, the MOSFET with the lower $V_{GS(th)}$ begins to conduct first during turn-on and therefore carries a larger portion of the current. During turn-off, the same device can remain conducting for longer and again experience a higher current while voltage is present across the device. Repeated exposure to this imbalance can reduce system efficiency and place additional stress on the affected semiconductor.

	Threshold voltage $V_{GS(th)}$ min/max	Threshold voltage tolerance max - min
	V	V
Comp A	3.5/5.7	2.2
Comp B	2.0/4.0	2
Comp C	1.8/3.6	1.8
Comp D	1.9/5.0	3.1
Comp E	3.5/5.7	2.2
Comp F	1.8/4.0	2.2
Comp G	1.8/4.3	2.5
Comp H	2.7/5.6	2.9
nexperia	1.7/2.9	1.2

Fig. 12 Comparison of $V_{GS(th)}$ ranges and threshold-voltage tolerances for Nexperia and competitor MOSFETs

As shown in Fig. 12, Nexperia 1200 V SiC MOSFETs specify a $V_{GS(th)}$ range of 1.7 V to 2.9 V (on the example of NSF040120L4A0), resulting in a worst-case threshold-voltage spread of only 1.2 V. This is considerably tighter than the spreads shown for the competitor devices and provides greater consistency in their switching behaviour. This inherently tight threshold voltage rends end of line devices classifications and additional expensive measurements unnecessary.

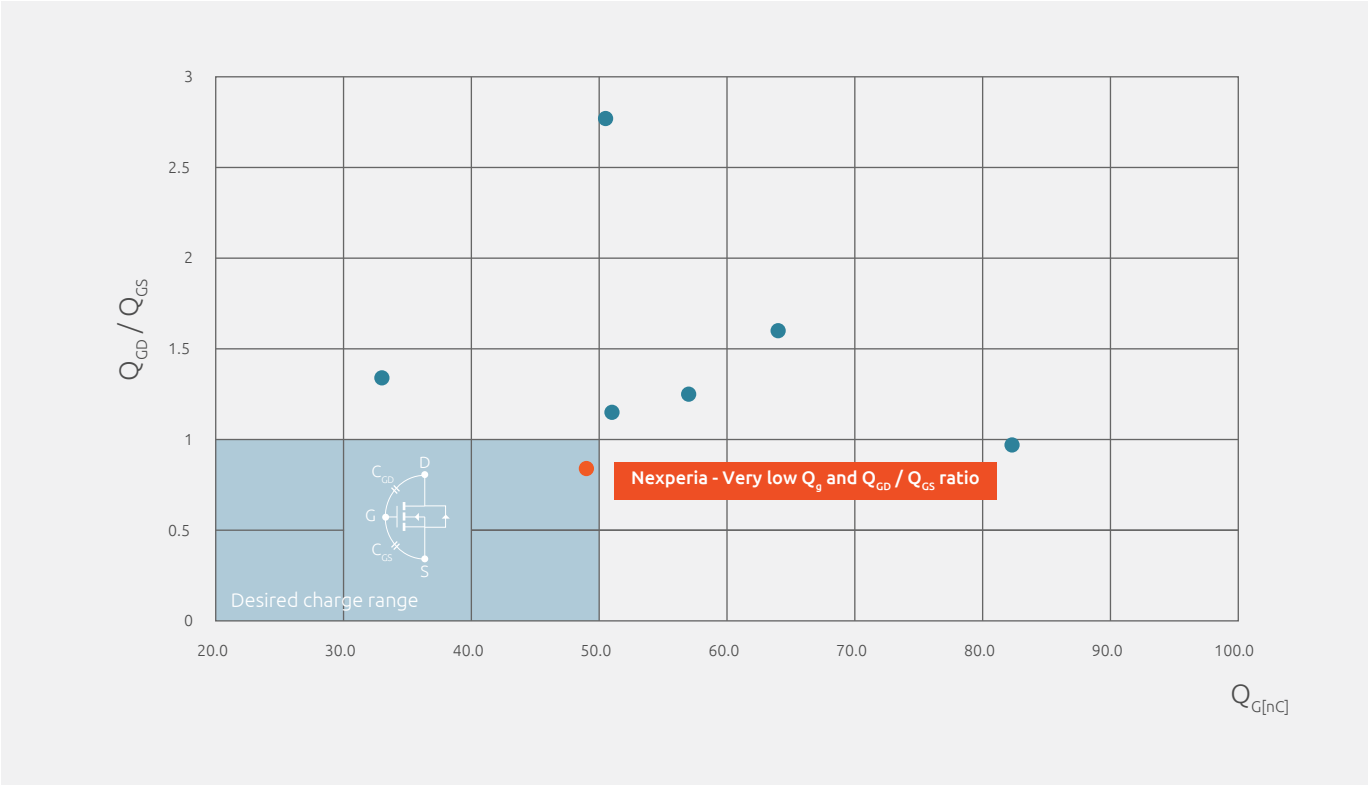


Fig. 13 Gate charge optimization for stable switching performance for 1200V SiC MOSFETs

The gate-drain to gate-source charge ratio, Q_{GD} / Q_{GS}, is an important indicator of switching robustness in MOSFETs. For stable operation, the gate-source charge should be sufficiently larger than the gate-drain charge, while the absolute gate charges should still remain low to support fast and efficient switching, as illustrated in Fig. 13.

This relationship is especially important for reducing the risk of parasitic turn-on. During turn-off, the drain-source voltage V_{DS} rises rapidly as the MOSFET begins to block voltage. This high dV/dt couples through the gate-drain capacitance C_{GD} and injects current into the gate. If the resulting gate-voltage transient becomes large enough to approach the gate-source threshold voltage, the MOSFET may partially turn on again even though the gate driver is commanding it off.

A low Q_{GD} / Q_{GS} ratio therefore helps keep the induced gate-voltage rise under control, improving immunity against unwanted turn-on. This supports safer and more stable switching, particularly in fast half-bridge applications where high dV/dt and tight dead times are common. Uncontrolled parasitic turn-on can cause cross-conduction, excessive current stress, and potentially catastrophic device failure.

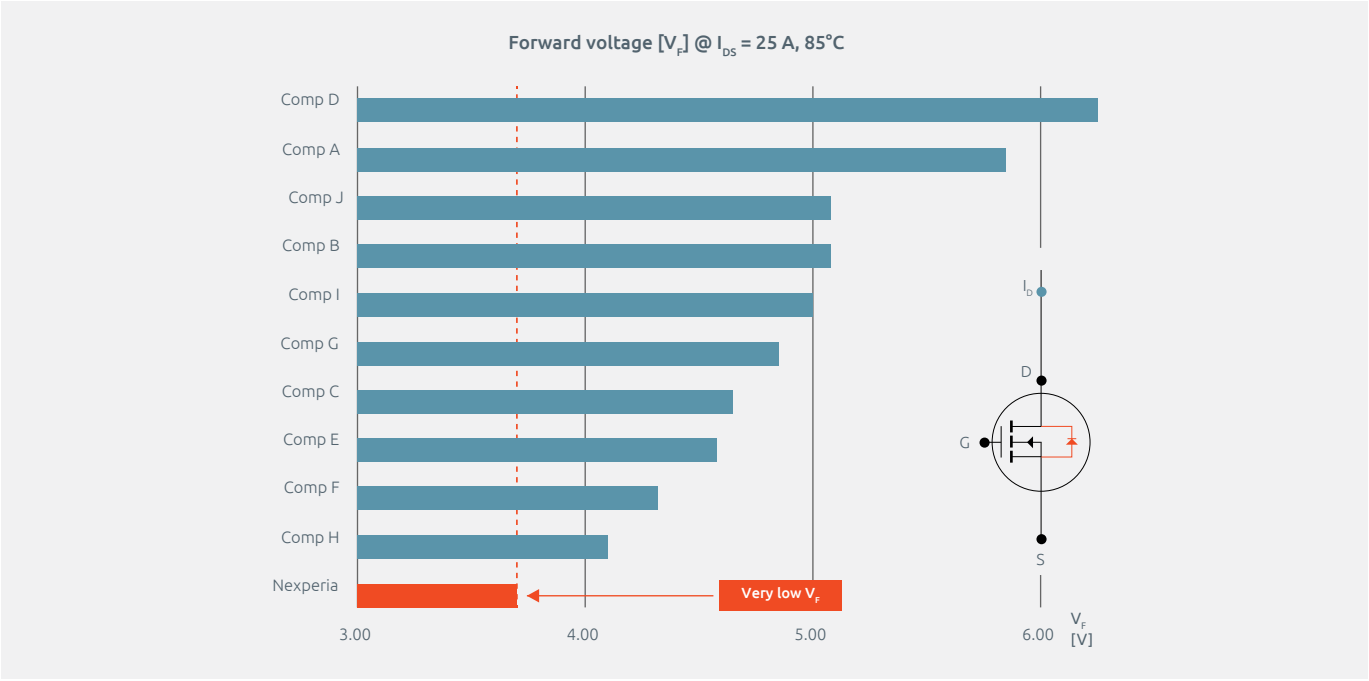


Fig. 14 Comparison of 1200 V SiC MOSFET body-diode forward voltage at 25 A and 85 °C.

As shown in Fig. 14, the body-diode forward voltage V_F is another important parameter, particularly in half-bridge topologies. During dead time, both the high-side and low-side MOSFETs are turned off to prevent cross-conduction. However, the current of an inductive load cannot change instantaneously, so it commutates through the body diode of the appropriate MOSFET. The instantaneous diode conduction loss can be approximated by:

$$P_{(diode,inst)} \approx V_F * I_D$$

Although the dead-time interval is typically only tens to hundreds of nanoseconds, the associated energy loss is repeated during every switching cycle. Consequently, at high switching frequency and high load current, body-diode conduction can contribute significantly to the total converter losses. Fig. 14 shows that the Nexperia 1200 V SiC MOSFET achieves a forward voltage of approximately 3.5 V at I_{DS} = 25 A and 85 °C, lower than the compared devices. This reduces dead-time conduction energy, thermal stress, and the overall cooling requirement.

A low reverse-recovery charge Q_{rr} is also advantageous because it reduces the current transient and switching energy during commutation of the body diode. The combination of low V_F, low Q_{rr}, low Q_{GD}/Q_{GS}, and low switching charge therefore enables lower switching losses, improved dV/dt robustness, higher switching-frequency capability, and more flexible dead-time optimization in high-performance SiC power converters.

		650/750 V	1200 V
SiC Schottky Diodes	Discretes	Available	Available
SiC MOSFETs	Discretes	Coming soon	Available
	Top Side Cooling		
SiC Modules	NexPack molded modules		On roadmap
	FlexPack frame modules		

4.3 Selecting low R_{DSon} GaN FET switches for best efficiency and EMC performance for PFC topologies.

Silicon carbide (SiC) devices are particularly well suited to high-voltage and high-power conversion stages, where robustness, thermal performance, and efficient switching are critical. This makes SiC an attractive technology for applications such as rectification, PFC stages, inverters, and other high-voltage power-conversion systems.

Low R_{DSon} GaN devices provide a complementary solution. In the 650 V voltage class, GaN combines low conduction losses with very fast switching capability, making it particularly attractive when higher switching frequencies and increased power density are required. The choice between SiC and GaN therefore depends strongly on the voltage level, switching frequency, thermal requirements, power level, and overall converter architecture. In better understanding the datasheet parameters application note AN90005 Understanding power GaN FET data sheet parameters can help.

An important consideration when comparing competing power-semiconductor technologies is that datasheet values and simulation results alone do not always provide a true like-for-like comparison. Device models are produced by different manufacturers using different modelling approaches, while datasheet parameters may also be measured under slightly different test conditions. Consequently, the most reliable comparison is obtained by evaluating the devices under the same electrical conditions and using the same hardware platform. For this reason, accurate device comparison starts with hardware evaluation.

Nexperia provides several evaluation platforms for this purpose. Double-pulse test boards are particularly useful for studying the dynamic switching behaviour of fast discrete devices. They allow evaluation of parameters such as turn-on and turn-off losses, switching transitions, reverse-recovery behaviour or overshoot and ringing to be compared under controlled conditions. All Nexperia GaN boards are optimised for lowest commutation loop inductance and are equipped with a high bandwidth current shunt for accurate current measurements. Double-pulse boards are available for different package and cooling configurations, including the latest released Gen 2 Cascode parts in a TOLL package, as shown on Fig. 16. In addition to double-pulse testing, the boards can be modified for continuous buck or boost converter operation, up to several kilowatts. For even higher power ratings of the converter the devices need to be parallelled. By using careful layout, short and impedance balanced gate drives, correctly placed DC bus snubbers and decoupling, it is possible to achieve excellent current sharing in paralleled GaN FETs driving an inductive load. Guidance with reference design and experimental results can be found in application note AN90030 Paralleling of Nexperia cascode GaN FETs in half-bridge topology.

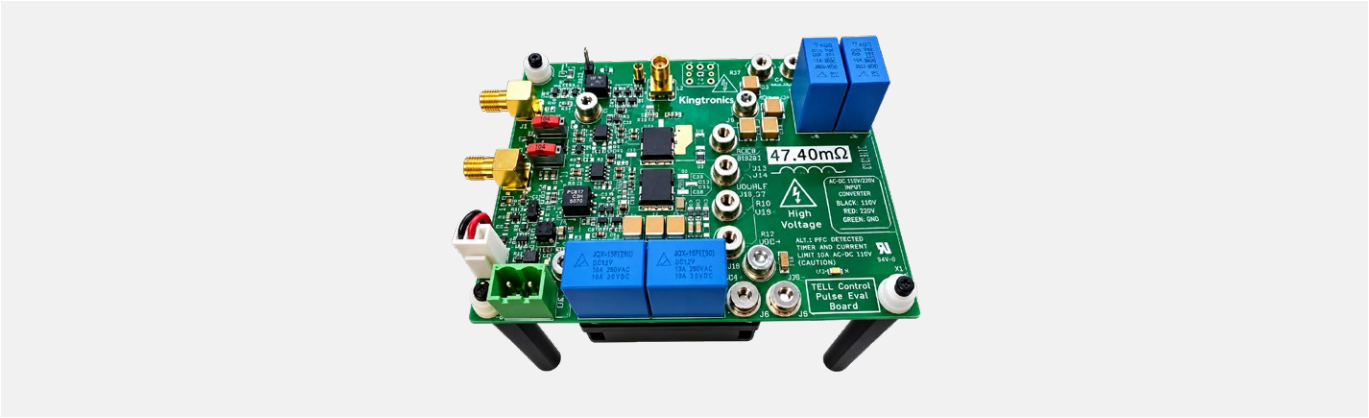


Fig. 16 Nexperia double pulse evaluation boards for low R_{DSon} GaN device in TOLL package.

The waveforms shown in Fig. 17 illustrate a comparison between first- and second-generation cascode GaN technologies. Both generations exhibit clean switching behaviour, but the second-generation device reduces the overlap between drain-source voltage and drain current during turn-on. Since instantaneous switching power is:

$$P(t) = V_{DS}(t) \times I_D(t),$$

reducing the duration and magnitude of this voltage-current overlap directly reduces the energy dissipated during the switching transition. In the example shown, this results in up to approximately 30% lower turn-on energy, while the turn-off losses remain similarly low.

Another important improvement is the reduction in reverse-recovery charge, Q_{rr}. The measured example shows approximately 33% lower Q_{rr} for the second-generation device. A lower reverse-recovery charge reduces the current transient associated with commutation and can therefore decrease switching stress, ringing, and the excitation of parasitic circuit elements. This is beneficial not only for efficiency but also for achieving cleaner switching behaviour and improving the converter's EMI/EMC performance.

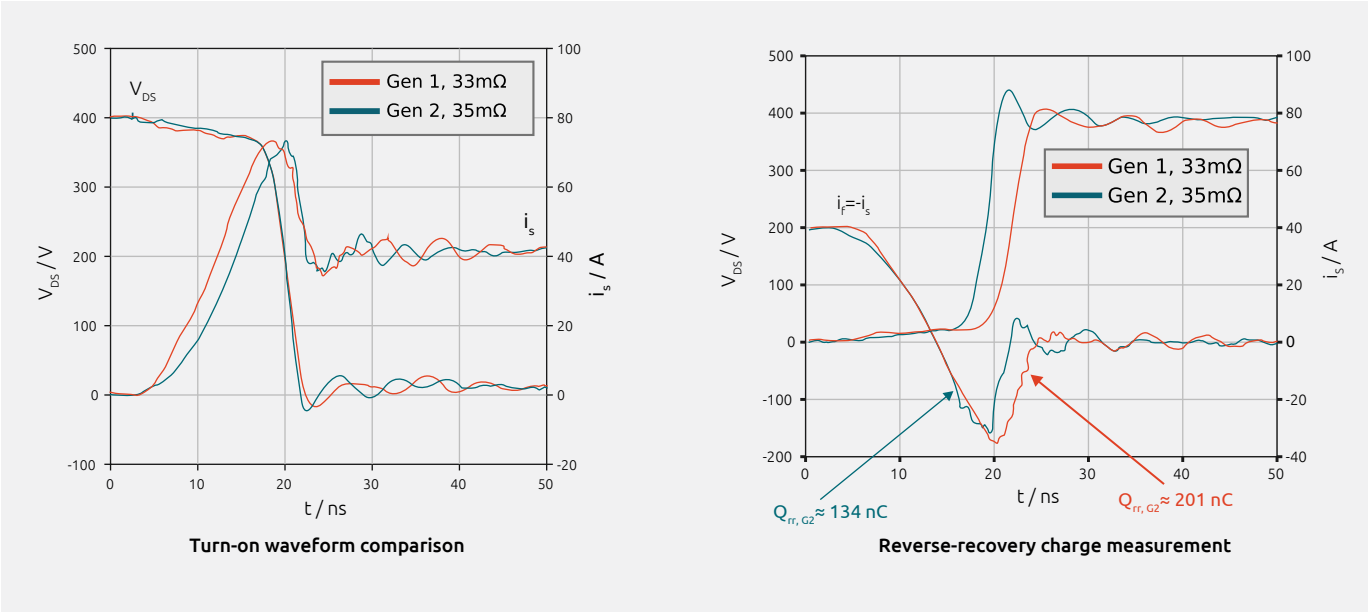


Fig. 17 Nexperia low R_{DSon} GaN Gen 1 and Gen 2 device switching performance comparison at 400 V, 40 A under typical application conditions

For more application-oriented evaluation, devices can be tested in a 4 kW, 85–265 Vac analog bridgeless totem-pole PFC platform. Such a board makes it possible to evaluate semiconductor performance under realistic converter conditions rather than considering isolated switching events. The implementation demonstrates a high efficiency solution with latest Cascode GaN FETs in a familiar industry-standard TOLL package, based on a low-cost analogue control approach.

TOLL PFC board

- TOLL devices provide pin-to-pin compatibility
- Gen. 2 GaN technology
- 35% die shrink enables the same $R_{DS(ON)}$ devices as CCPAK1212, with better switching performance
- High efficiency with simple and low-cost analogue control

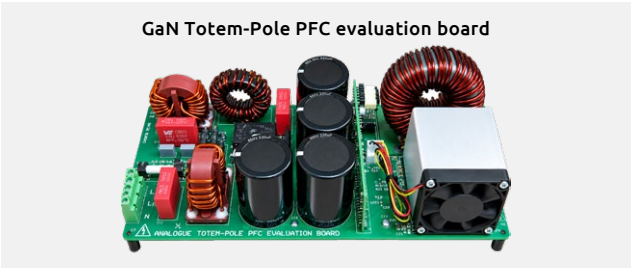


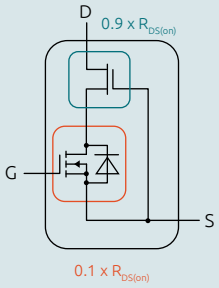
Fig. 18 Nexperia low RDSon GaN device totem-pole PFC evaluation board

5. Design challenges in UPS (BBU) and IBC

5.1 Selecting power semiconductor switches for DC/DC converters

The devices considered up till this point were low R_{DSon} GaN devices. These are high-power-oriented 650 V GaN implementations with wide gate-drive margin and low reverse-conduction loss.

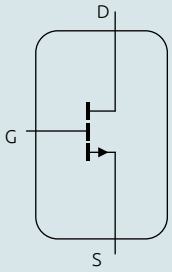
Suggested Nexperia Low R_{DSon} GaN devices



- $R_{DS(ON)}$ stability over temperature
- Higher saturation current
- Lower reverse-conduction losses
- Very low Q_{rr}
- Easy gate-drive design with a 0 to 12 V drive range
- Suited both for bootstrap and isolated driver supply

Fast switching GaN FETs on the other hand are normally-off GaN switches optimized for very high switching frequency and low stored charge.

Suggested Nexperia fast switching GaN FETs



- Normally-off power switch with lowest Q_g
- Ultra-high switching frequency capability
- Leading soft-switching performance
- No minority carrier reverse-recovery charge
- Low gate charge and low output charge
- Lowest switching delays
- High performance (>99% efficiency in the cited application context)
- Simple 0 to 5/6 V gate drive
- Suitable for low-voltage and high-voltage low / mid-power applications

Comparison of various GaN technologies can be found in Nexperia_GaNFETs. An overview of Nexperia low R_{DSon} and fast switching 650V GaN devices is provided in Table 2.

	DPAK	DFN5060	DFN8080	TO-247 3L	TO-247 4L	TOLL	TOLT
R_{dson} typical (mΩ)							
35				GAN041-650WSB	GANC035-650VSH	GANC035-650TBH	GANC035-650UTH
50				GANC050-650WSH	GANC050-650VSH	GANC050-650TBH	GANC050-650UTH
60			GAN080-650EBE				
70				GANC070-650WSH		GANC070-650TBH	GANC070-650UTH
106	GANE140-700BBA	GAN140-650FBE	GAN140-650EBE				
138	GANE190-700BBA	GAN190-650EBE	GAN190-650FBE				
165	GANE240-700BBA						
270	GANE350-700BBA	GANE350-650FBA					
	Fast switching	Fast switching	Fast switching	Low R_{DSon}	Low R_{DSon}	Low R_{DSon}	Low R_{DSon}

Table 2 Nexperia GaN high voltage (650 V) portfolio – Industrial Grade

GaN fast switching devices are well suited to a range of high-frequency DC/DC converter topologies, with the optimum topology depending largely on the required power level and voltage conversion ratio. For lower-power auxiliary supplies (20-250 W), flyback converters (Fig. 19) remain attractive because of their simple implementation and their ability to provide multiple secondary outputs from a single transformer. This is particularly useful when several isolated supply rails are required.

At higher power levels, LLC resonant converters (Fig. 20) are more commonly used in the main power-conversion path. Their soft-switching operation allows GaN devices to exploit high switching frequencies while maintaining high efficiency and low switching losses. Typical applications include server and accelerator power supplies, with conversion stages such as 400 V ⟶ 48 V or 12 V and 48 V ⟶ 12 V.

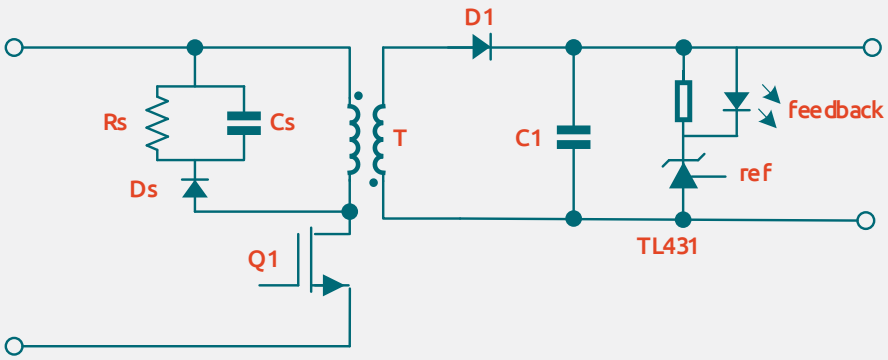
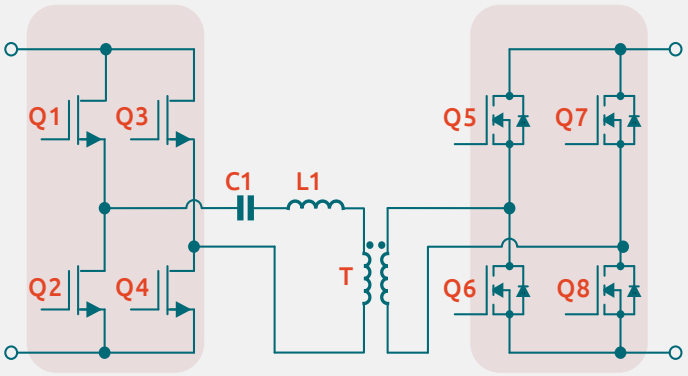


Fig. 19 Flyback converter - Low-power isolated DC/DC topology



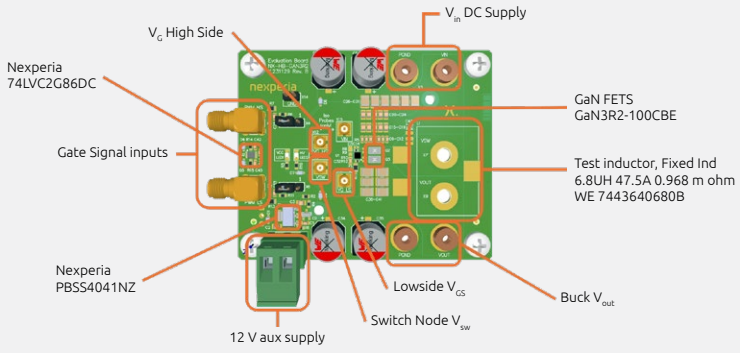
Power 250 W - several kW
Efficiency ~98%
Frequency Up to 300 kHz/500 kHz+
Switching Soft switching

Typical applications
- High-power servers
- Accelerator PSUs
- 400 V → 48V/12V
- 48 V → 12 V

Key advantage: Very high efficiency at high power density

Fig. 20 LLC resonant converter - High-efficiency resonant DC/DC topology

The 60 V, 350 W fast switching GaN half-bridge evaluation board provides a practical platform for investigating these high-frequency DC/DC applications and is especially relevant to data-centre power architectures. Importantly, the associated design files are available, allowing engineers to reproduce, modify and adapt the design to their own application.



Input up to 60 V
Power 350 W
Efficiency ~98%
Frequency typ. 250–750 kHz
Key features
- Very low parasitic inductance
- Buck or boost operation
- Internal dead-time control
- MMCX V_{GS} and V_{DS} sensing
- Replaceable inductor connection

Key advantage: Compact platform for very-high-frequency DC/DC development

Fig. 21 Fast switching GaN half-bridge evaluation board - High-frequency GaN evaluation platform

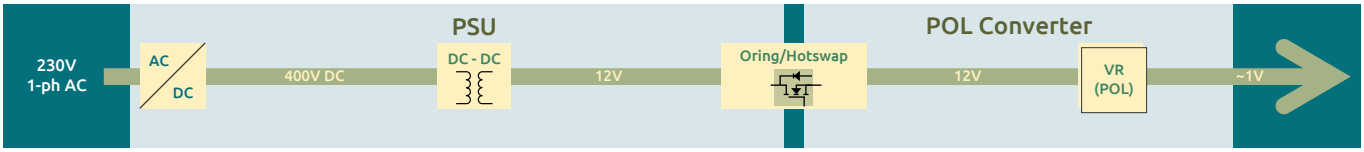
Further guidance on fast switching GaN gate drive design can be found in application note AN90041 Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs.

At the heart of the 48 V backbone of the rapidly increasing power levels of server racks, the 100 V GaN device class provides the optimal balance between rail margin, switching speed and power density. Nexperia's medium voltage GaN FETs deliver over 98% peak efficiency, up to 5× higher switching frequency and up to 70% smaller footprint compared to silicon, enabling smaller magnetics, reduced PCB area and lower cooling requirements when used in BBU and IBC. Low voltage GaN devices (15–60 V) complement this by powering high current Point of Load (POL) and Voltage Regulator Module (VRM) stages with fast transient response and minimal conduction losses. Across both voltage classes, top side cooled (TSC) packages ensure efficient heat removal in space constrained environments. Presented in Table 3, Nexperia's LV and MV GaN portfolio provides a scalable, thermally robust and high density platform for next generation AI datacenter power systems, supporting PSU, IBC, DC/DC and compute rail conversion with industry leading efficiency and size reduction.

		WLCSP	FCLGA	VQFN7 (QFN4x6)	PQFN3x5 TSC	PQFN3.3x3.3 TSC (2 versions)	PQFN3.3x2.6 TSC
Voltage	Rdson typical [mΩ]						
15 V	0.3					GANE0R3-015QTL	
25 V	0.4					GANE0R4-025QTL	
40 V	0.5					GANE0R5-040QTL	
	0.8						GANE0R8-040QTL
80 V	8.5	GANE011-080CBA					
100 V	0.75				GANE0R8-100QTM		
	1.2					GANE1R2-100QTM	
	1.4			GANE1R8-100QBA			
	2.1	GANE2R7-100CBA					
	2.4	GAN3R2-100CBE					
	5.5	GANE7R0-100CBA					
150 V	3.2			GANE3R9-150QBA			
	5.6		GAN7R0-150LBE				
200 V	3.5				GANE3R5-200QTM		
	7.2				GANE7R2-200QTM		

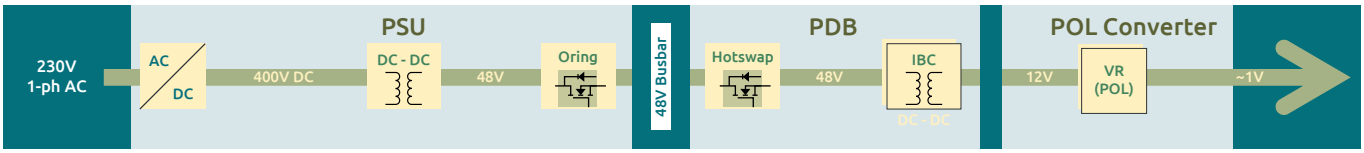
Table 3 Nexperia GaN Low and Medium-voltage (15 V – 200 V) Portfolio – Industrial Grade

Conversion to low (48 V or 12 V – see reference design board) voltages are performed in the Power Delivery Board (PDB) within the server tray in future 400/800 V power distribution architectures and in the rack in the existing 48 V architectures. Further conversions to multiple power rails at 12 V, 5 V and 3.3 V follow within the motherboard. These power rails are distributed with or without galvanic isolation to various loads that include cooling fans, NIC modules, HMI and local storage. Finally, core voltage level (0.8-1.8 V) at high currents are achieved with paralleled half bridge MOS or GaN FET converters with integrated gate drivers and newly also integrated magnetic elements, close to the server MCU or accelerator GPU. Please see Fig. 22 and Fig. 23 for suggested MOSFETs for these power conversion stages.



12 V Bus	DC/DC Secondary	Oring / Hotswap
Function	Sync. Rectification	Power Switch / Hotswap
R_{DSon}	< 2 m	< 2 m
BV_{Dss}	40 V/60 V	25 V/30 V
Packages	5x6	5x6 / 3X3
Part #1	PSMN1R0-40YLD	PSMNR51-25YLH/R58-30YLH
Part #2	PSMN1R4-40YLD	PSMN0R7-25YLD
Part #3	-	PSMN1R0-30YLC/D
Part #4	-	PSMN1R6-30MLH

Fig. 22 Traditional power architecture with no power shelf & with 12 V bus



48 V Bus	DC/DC Sec.	Oring	Hotswap	IBC	BBU	BBU
Function	SR	Power Switch	Hotswap	DC/DC/ SR	Power Switch	DC/DC
R_{DSon}	< 5 m	< 5 m	< 5 m	< 3 m	1 m – 3 m	> 5 m
BV_{Dss}	80 V	80 V	100 V	80 V + 60 V	100 V	100 V
Packages	5x6	5x6	8x8 / >10x10	5x6/5x6 DSC	8x8 / >10x10	5x6
Part #1	PSMN2R6-80YSF	PSMN2R6-80YSF	PSMN2R3-100SSE	PSMN2R6-80YSF	PSMN2R0-100SSF	PSMN9R8-100YSF
Part #2	PSMN3R3-80YSF	PSMN3R3-80YSF	PSMN4R8-100Y/BSE	PSMN3R3-80YSF	PSMN1R0-100ASF	PSMN7R2-100YSF
Part #3	PSMN3R5-80YSF	PSMN3R5-80YSF	PSMN1R0-100A/CSE	PSMN3R5-80YSF	PSMN1R3-100ASF	PSMN5R5-100YSF

Fig. 23 Current power architecture with power shelf & 48 V Bus

As switching frequencies increase, traditional Schottky rectifiers increasingly become a source of power loss, heat generation and EMI. In high-frequency converters, reverse recovery charge (Q_{rr}), peak reverse recovery current (I_{rrm}), switching losses and thermal stress become just as important as forward voltage drop (V_F). This is particularly true for AI server power systems operating at frequencies between 250 kHz and 2.2 MHz, where efficiency gains of even a fraction of a percent translate into significant reductions in datacenter energy consumption and cooling requirements.

Product Name	Package	Rated Voltage	Rated Current
PMEG100Y10ELXD(-Q)	CFP2-HP	100 V	1 A
PMEG100Y20ELXD(-Q)			2 A
PMEG100Y20ELXE(-Q)	CFP3-HP	100 V	2 A
PMEG100Y30ELXE(-Q)			3 A
PMEG100Y10ELR(-Q)	CFP3	100 V	1 A
PMEG100Y20ELR-Q			2 A
PMEG100Y30ELR-Q			3 A
PMEG100Y50ELP-Q	CFP5	100 V	5 A
PMEG100Y080ELPE-Q	CFP15B	100 V	8 A
PMEG100Y100ELPE-Q			10 A
PMEG100Y120ELPE-Q			12 A
PMEG100Y150ELPE-Q			15 A
PMEG100Y200ELPE-Q			20 A

Table 4 Nexperia Trench Gen2 100 V portfolio overview

Nexperia Trench Gen2 100 V Schottky diodes were developed specifically for high-frequency, efficiency-driven applications within the growing 48 V ecosystem. Key technology advantages include:

- Very low reverse recovery charge (Q_{rr})
- Reduced reverse recovery current (I_{rrm})
- Reduced turn-off energy (E_{off})
- Shorter reverse recovery time (t_{rr})
- Low leakage current at elevated junction temperatures
- Optimized balance between V_F and switching performance

Fig. 24 compares the reverse recovery behaviour of a 3 A, 100 V planar Schottky rectifier to a Nexperia Trench Gen2 Schottky. Trench Gen2 offers superior performance in reverse recovery behaviour in terms of reduced reverse recovery time (t_{rr}), reverse recovery charge (Q_{rr}) and peak reverse recovery current (I_{rrm}), improving switching speed as well as minimizing switching losses and stress on the MOSFET. The reduced turn-off energy (E_{off}) increases system efficiency and lowers the device temperature for easier cooling.

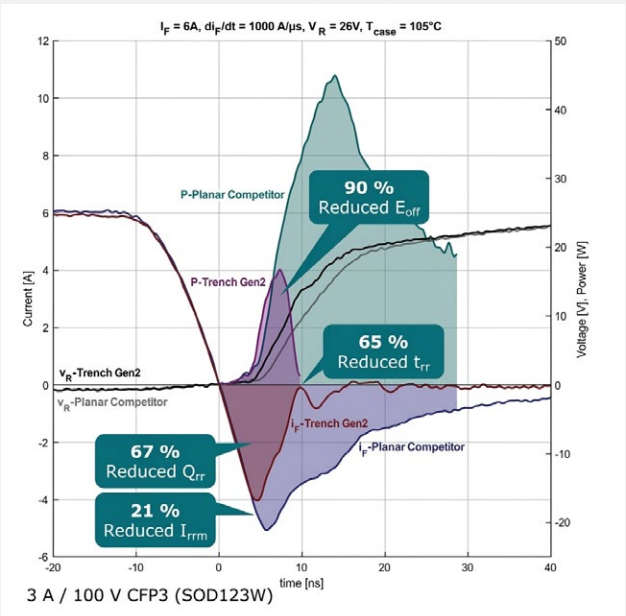


Fig. 24 Nexperia Trench Gen 2 Schottky diodes reverse recovery analysis

5.2 Maintaining power line integrity while hot-swapping modules

In order to have subsystems removed from the datacenter architecture, the input of the removed parts needs to have a hot swap controller. These controllers ensure that the disconnection and connection of the equipment does not damage the wider power supply in the vicinity of the replaced part. The two most demanding scenarios are therefore input capacitance charging at component startup and disconnection of fault current in the event of an output short circuit. Because of the amount of current and nature of the faults the hotswap controller needs to control external MOSFETs, as shown in Fig. 25. Indeed, the power levels requirements of modern datacenter IT shelves can approach 200 A, requiring MOSFET paralleling. The described operation states require the paralleled MOSFETs to share load in the linear and avalanche operation modes.

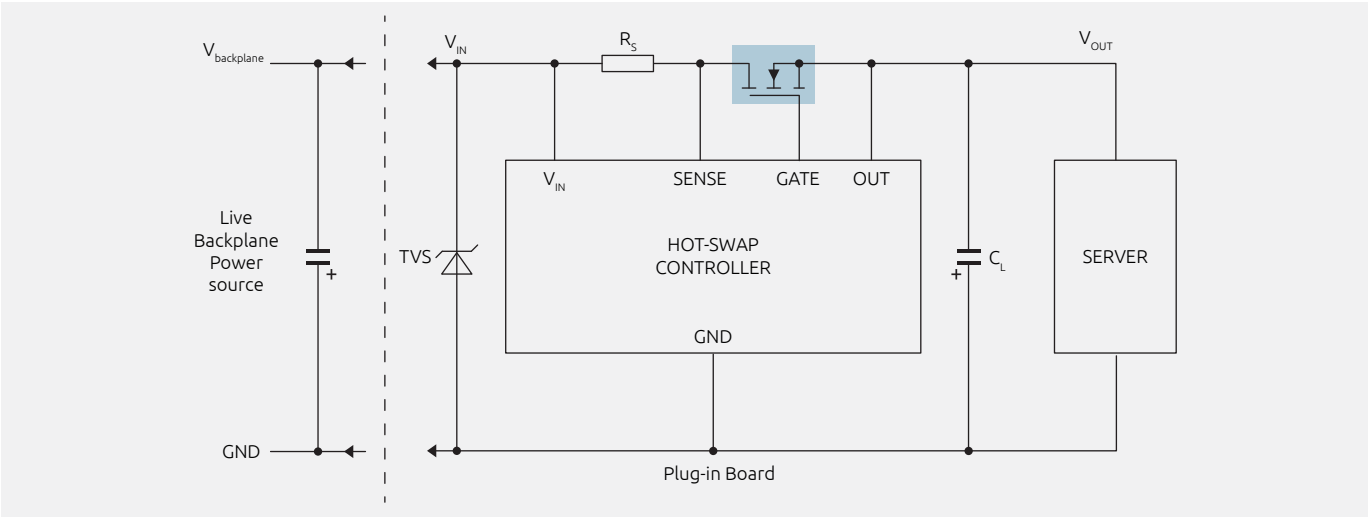


Fig. 25 Hot swap controller with external MOSFET

The best way to appreciate the challenges is to investigate a reference design (TI 48V, 8kW, Analog Devices 54V, 72A). In Fig. 26 a reference design board is depicted with TI LM5066I hot-swap controller controlling nine LFPAK88 PSMN2R3-100SSE Nexperia Application Specific MOSFET devices for Hotswap and Soft Start. The system can handle currents up to 150 A with an output voltage of 54 V with a 60°C maximal MOSFET top temperature in a 25°C ambient. The challenges of a startup and over current event are illustrated in Fig. 27. At startup the current is limited to 1 A, resulting in over 50 W of losses in the MOSFETs as they block the full input voltage at the beginning of the event. This power dissipation decreases as the input capacitors of 4.2 mF fill up with charge and take over the voltage. This amount of power dissipation needs to be distributed among several MOSFETs due to their limited cooling arrangements. Similarly, in the turn off transient of the overcurrent event, the large current needs to be shared between the nine MOSFETs. MOSFETs are known to share power dissipation well in conduction mode as their R_{DSon} has a positive temperature coefficient. This means that in conduction mode the MOSFET that carries the largest amount of current gets hotter, its R_{DSon} increases and thus balances out with the rest of the devices in parallel. However, the power sharing in transient modes such as linear mode and switching transitions this is proving to be a challenge, needing special silicon technologies (AN50005 Paralleling power MOSFETs).

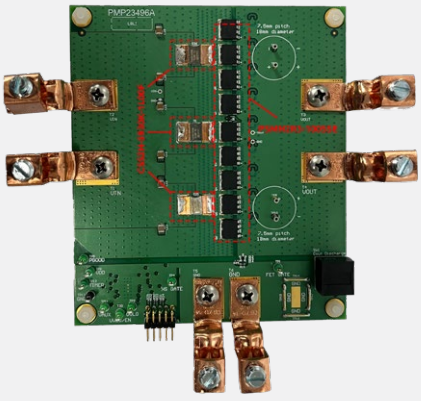


Fig. 26 8 kW hot-swap reference design for AI servers - TI 48 V, 8 kW

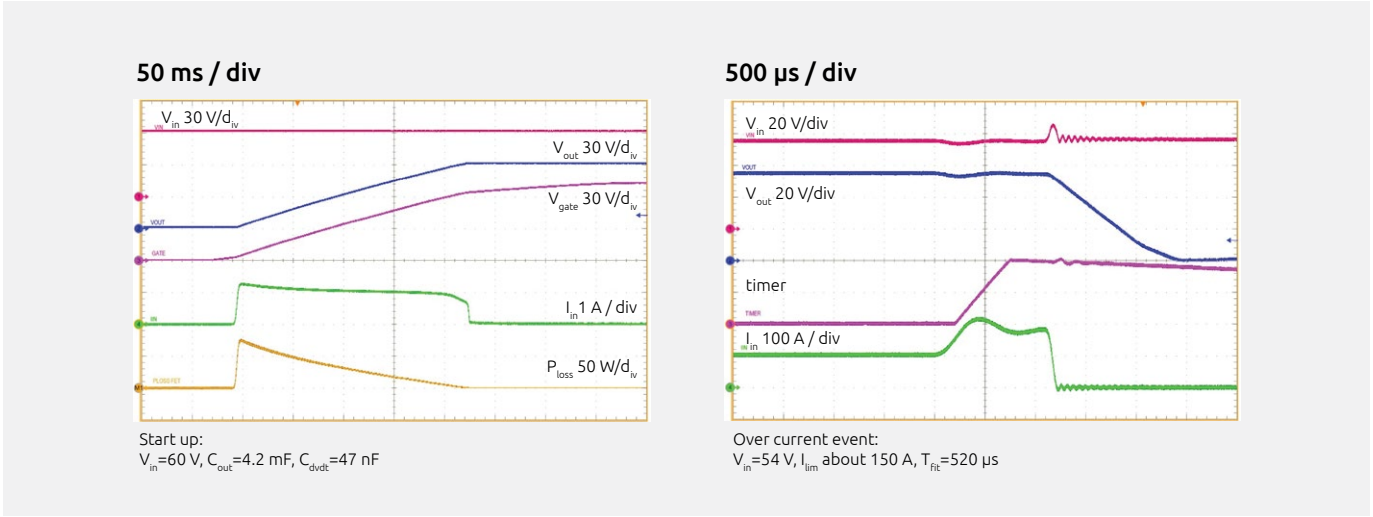


Fig. 27 Startup and overcurrent shutdown event handling - TI 48 V, 8 kW

Choosing a hot-swap MOSFET (AN90081 How to pick a hot-swap MOSFET) encompasses the usual voltage and current ratings. For safety reasons the margin between the MOSFET breakdown voltage and the input voltage should be 1.5 to 2 fold. A bit of caution needs to be raised around general MOSFET current rating choices. The current rating from the datasheet is conducted under extreme cooling arrangements and therefore is not much use for immediate comparison with current requirements of the application. Instead, designers need to start from the allowed power dissipation for the MOSFET (a rule of thumb for LFPAK56 on FR4 is about 1 W, scales with package size and PCB material). The square of the current can be obtained by dividing the power dissipation with the maximal R_{DSon} at the highest expected temperature of the die (usually twice the room temperature value).

Next, hot-swap MOSFET specific SOA needs to be taken into account (How to pick a hot-swap MOSFET). In Fig. 28 the background is the SOA of a regular MOSFET with same package and voltage rating as well as comparable R_{DSon} . At higher voltage a slight knee can be seen in all the characteristics, cutting down the MOSFET capabilities. This is due to a so called 'Spirito effect' that occurs because of hotspots occurring on the MOSFET die due to the negative temperature coefficient of the V_{GSth} of the MOSFET trenches, causing thermal runaway. The Hotswap Application Specific FET (ASFET) technology does away with this effect and therefore the knee on the graph as well. This is illustrated with the example of the 100 ms characteristics noted in red line. Because of the absence of the knee on the characteristics the ASFET can conduct 4 times higher current for 100 ms at 50 V drain to source voltage.

A further note to the SOA characteristic in general (both ASFETs and regular MOSFETs) is that they are measured using rectangular power pulses, while in reality the pulses are triangular due to the changing nature of either the current or voltage of the device (depending if the load is inductive or capacitive). Due to this the actual allowed peak current through the device can be twice as high as noted on the SOA (so 4 A and 16 A on the example of Fig. 28, see AN50019 - Thermal boundary condition study on MOSFET packages and PCB substrates).

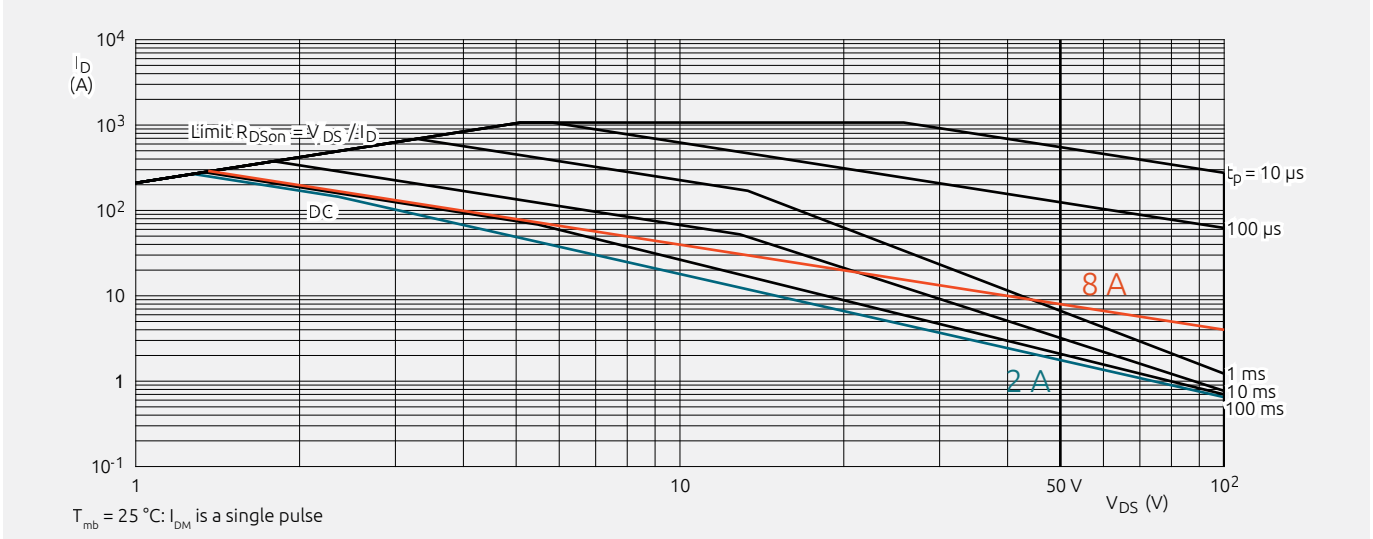


Fig. 28 Hotswap ASFET SOA compared to regular technologies

When paralleling, MOSFETs size is certainly of significance. The designer's choice should be increasing the MOSFET package and cooling arrangements as far as permissible. Once paralleling becomes necessary the number of MOSFETs parallelled should be minimised to reduce the challenges of turning them on and off at the same time. This includes equal cooling arrangements, distributed gate resistors, equidistant gate traces, etc. The larger the number of MOSFETs paralleled, the larger the margins needed for safe operation, further increasing the number of MOSFETs. This is illustrated on Fig. 29 for the current and next generation datacentre hot-swap requirements. Looking at the reference design power rating of 7.5 kW , it can be noticed that the requirement is converted with 9 8x8 mm devices or only 5 12x12 mm ones and just 4 inverted 12x12 mm packages.The occupied PCB area is around 650 mm^2 for the 8x8 and 12x12 inverted devices and around 800 mm^2 for the inverted 12x12 devices.

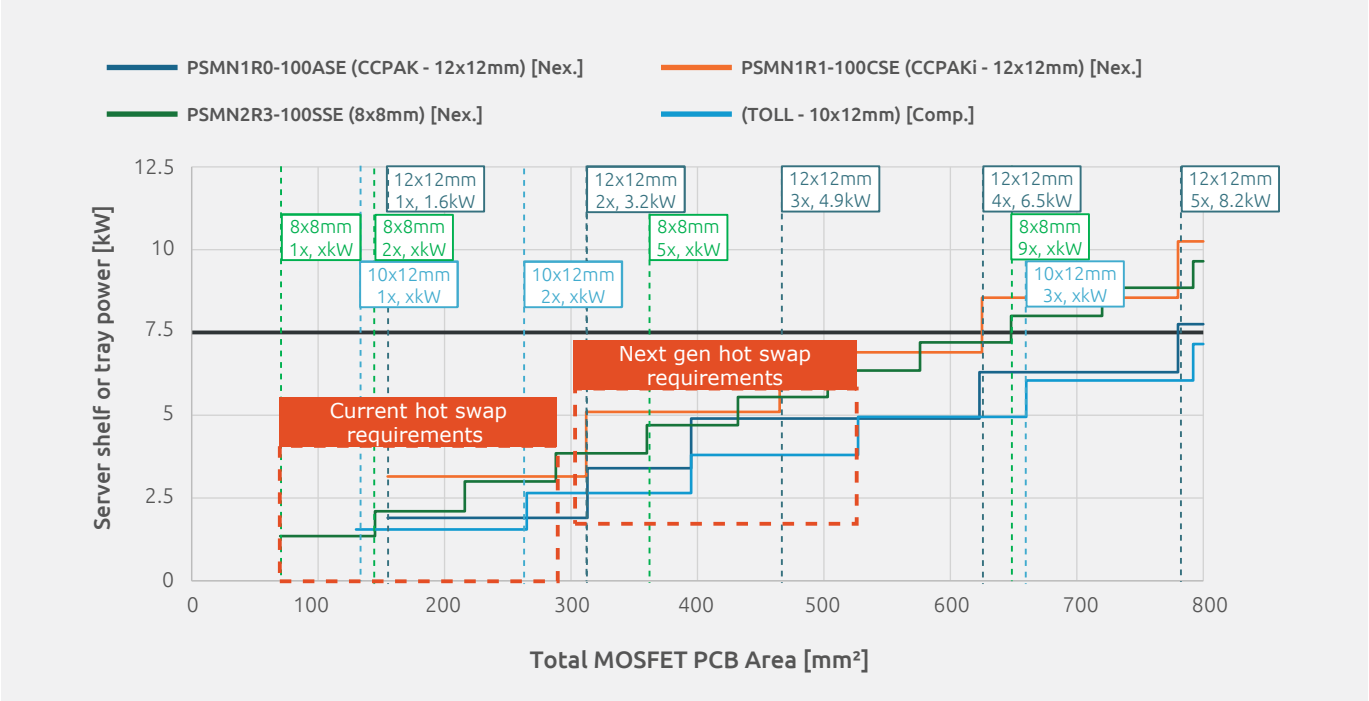


Fig. 29 Power density comparison of paralleled MOSFETs in different packages – LFPAK88, TOLL and CCPAK1212

Hot-swap ASFETs also hide a trick in their sleeve related to turn on speed related to V_{gs} threshold, which is shown in Fig. 30, comparing transfer characteristics of regular (red curves) and two ASFET MOSFET technologies (blue and green curves). With all three characteristics the difference between the full and dotted lines might be because of characteristic differences within the technology limits or difference because of die temperature of the MOSFETs. In either case, the current difference for a certain voltage level (4 V noted on the figure) is high in the regular, fast turn on MOSFETs and limited with the ASFET technologies. This means there is less discrepancy between the current levels handled by the individual MOSFETs and expensive end-of-line MOSFET parameter filtering or MOSFET parameter matching is avoided.

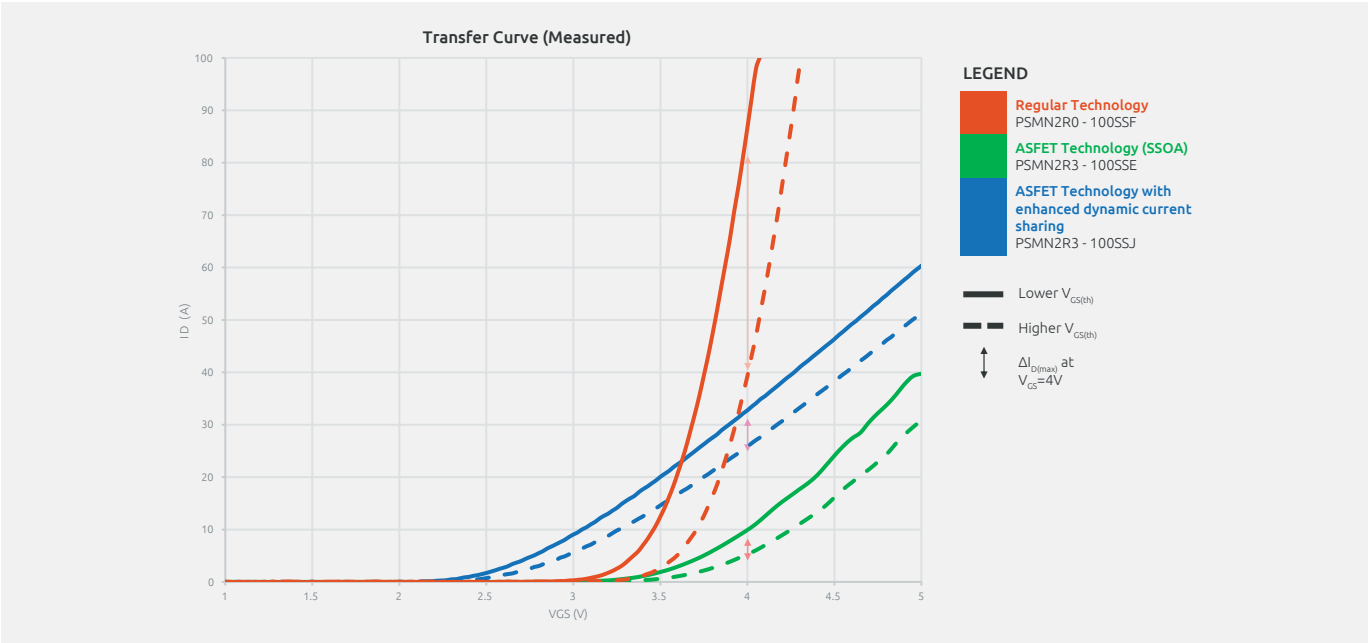


Fig. 30 Slower drain current rise with gate voltage improves paralleling mismatch

Further study, advice and guidance to MOSFET paralleling can be found Paralleling power MOSFETs in high power applications.

For lower power loads the protection device does not need to be parallelled or indeed external. Input protection controllers can contain the switching device itself as well. Such devices are called eFuses and their functionalities is to protect the load from input voltage spikes and the upstream power supply from hot-plugging, startup inrush currents, overload currents and reverse currents. Other functionalities include:

- Protecting the input power supply from load faults
- Built in soft start
- Adjustable over current limit
- Reverse current protection
- Output short circuit protection
- Over temperature protection
- Undervoltage lockout
- Overvoltage clamping
- Programmable output slew rate
- Quick output discharge

As demonstrated in Fig. 31 eFuses can be positioned at the entry point of the motherboard itself, but also at plug in boards like memory, hard drives, and fans. Nexperia NPS3102A/B can be evaluated on the boards: NEVB-NPS3102A 12 V, 2-13.5 A, 17 mΩ latching eFuse evaluation board and NEVB-NPS3102B 12 V, 2-13.5 A, 17 mΩ auto-retry eFuse evaluation board. for the 12V rail. A more comprehensive NPS210x family integrates a low-resistance pass FET, programmable current limiting, soft-start control, thermal protection, and flexible fault-management capabilities into a compact footprint, operating from 2.7 V to 21 V with adjustable current limits from 0.5 A to 5 A, can also be considered to support 3.3 V, 5 V, and 12 V power rail architectures.

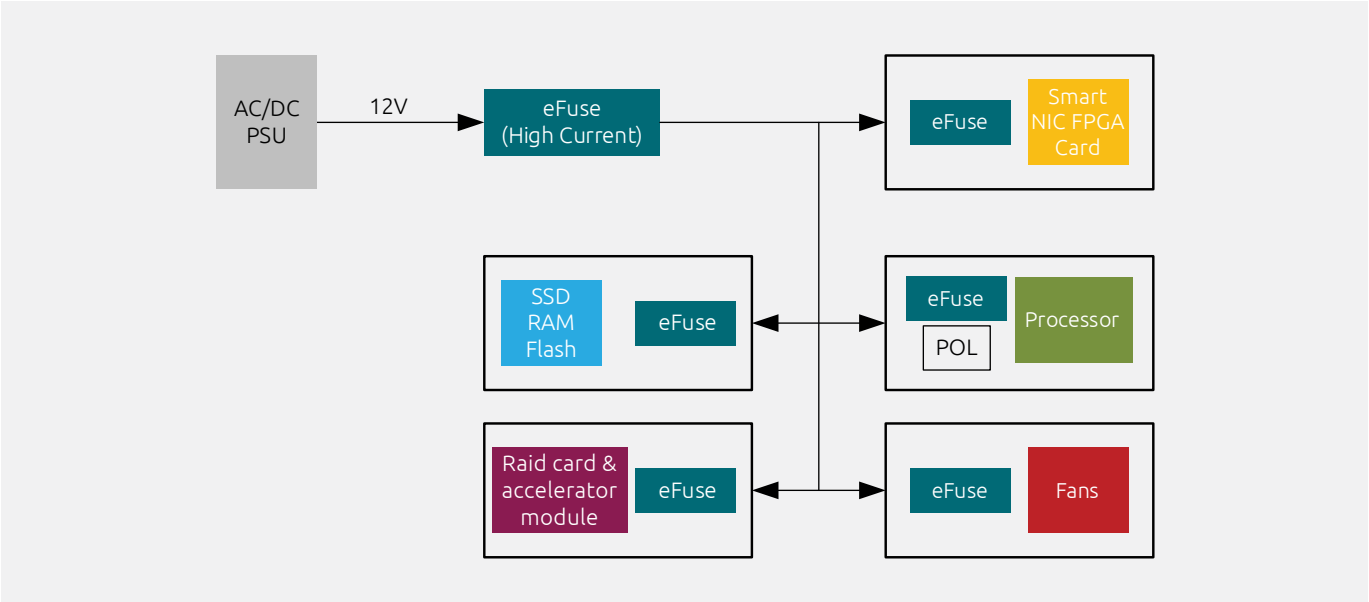
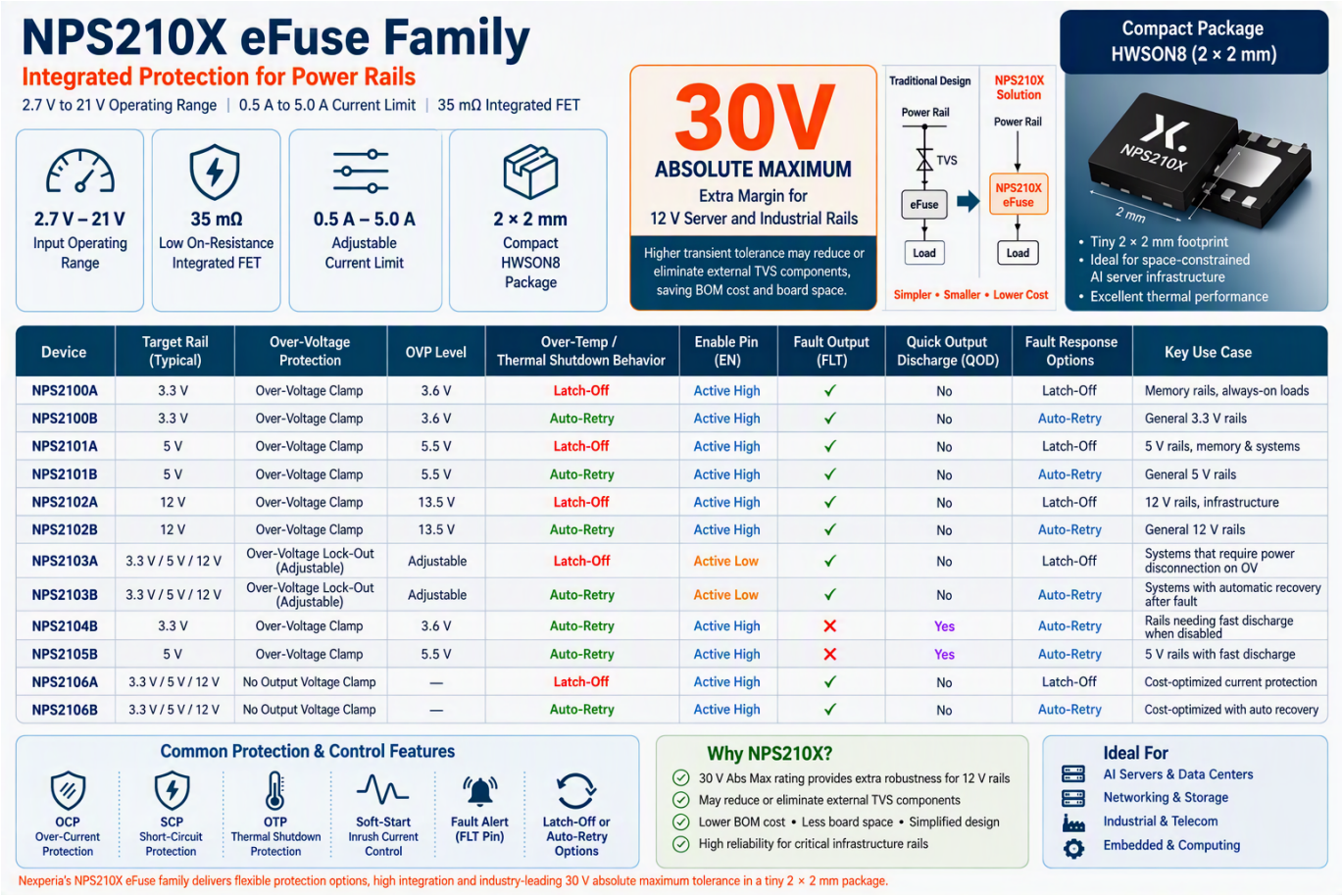


Fig. 31 eFuse application diagram for servers



Device	Target Rail (Typical)	Over-Voltage Protection	OVP Level	Over-Temp / Thermal Shutdown Behavior	Enable Pin (EN)	Fault Output (FLT)	Quick Output Discharge (QOD)	Fault Response Options	Key Use Case
NPS2100A	3.3 V	Over-Voltage Clamp	3.6 V	Latch-Off	Active High	✓	No	Latch-Off	Memory rails, always-on loads
NPS2100B	3.3 V	Over-Voltage Clamp	3.6 V	Auto-Retry	Active High	✓	No	Auto-Retry	General 3.3 V rails
NPS2101A	5 V	Over-Voltage Clamp	5.5 V	Latch-Off	Active High	✓	No	Latch-Off	5 V rails, memory & systems
NPS2101B	5 V	Over-Voltage Clamp	5.5 V	Auto-Retry	Active High	✓	No	Auto-Retry	General 5 V rails
NPS2102A	12 V	Over-Voltage Clamp	13.5 V	Latch-Off	Active High	✓	No	Latch-Off	12 V rails, infrastructure
NPS2102B	12 V	Over-Voltage Clamp	13.5 V	Auto-Retry	Active High	✓	No	Auto-Retry	General 12 V rails
NPS2103A	3.3 V / 5 V / 12 V	Over-Voltage Lock-Out (Adjustable)	Adjustable	Latch-Off	Active Low	✓	No	Latch-Off	Systems that require power disconnection on OV
NPS2103B	3.3 V / 5 V / 12 V	Over-Voltage Lock-Out (Adjustable)	Adjustable	Auto-Retry	Active Low	✓	No	Auto-Retry	Systems with automatic recovery after fault
NPS2104B	3.3 V	Over-Voltage Clamp	3.6 V	Auto-Retry	Active High	✗	Yes	Auto-Retry	Rails needing fast discharge when disabled
NPS2105B	5 V	Over-Voltage Clamp	5.5 V	Auto-Retry	Active High	✗	Yes	Auto-Retry	5 V rails with fast discharge
NPS2106A	3.3 V / 5 V / 12 V	No Output Voltage Clamp	—	Latch-Off	Active High	✓	No	Latch-Off	Cost-optimized current protection
NPS2106B	3.3 V / 5 V / 12 V	No Output Voltage Clamp	—	Auto-Retry	Active High	✓	No	Auto-Retry	Cost-optimized with auto recovery

Fig. 32 NPS210x eFuse family

5.3 Protecting the AI datacenter power conversion chain against surge and overvoltage events

As AI datacenters continue their transition toward higher power density and rack-level power delivery, the electrical infrastructure is evolving from traditional AC distribution toward 48 V, 400 V and even 800 V DC architectures. Every stage in the power delivery path, from the facility entrance to the processor core, is exposed to surge, load-dump and transient overvoltage events that can threaten system reliability and uptime.

The challenge for system designers is to implement surge protection that is robust enough to withstand the energy levels present at each power conversion stage, while maintaining efficiency, power density and thermal performance. Protection devices must coordinate with power semiconductors, converters and control electronics to prevent catastrophic failures without introducing excessive leakage currents, parasitic losses or PCB area requirements.

As rack power levels continue to rise, transient energy can no longer be treated as a front-end problem only. Protection must be deployed throughout the power delivery architecture:

- Utility and rack-level power entry
- Rectifier and PFC stages
- High-voltage DC buses
- 48 V intermediate buses
- 12 V power distribution rails
- Point-of-load converter inputs

Each location presents different surge amplitudes, operating voltages and energy handling requirements. A coordinated protection strategy therefore requires multiple classes of TVS solutions ranging from compact board-level devices to multi-kilowatt surge suppressors.

Suggested Nexperia TVS devices			
Power Conversion Stage	**Typical Voltage**	**Protection Requirement**	**Suggested Nexperia Devices**
Intermediate Bus Converter (IBC)	48 V	600-1500 W TVS protection	PTVS54VS1UR, PTVS58VS1UR, PTVS64VS1UR (CFP3/CFP5 families)
48 V Power Distribution	48-60 V	Board-level surge suppression	PTVS54VP1UP, PTVS58VP1UP, PTVS64VP1UP
12 V VRM Input Protection	12 V	400-600 W TVS protection	SMAJ12A, SMBJ12A, PTVS12VS1UR
Point-of-Load Rails	5-24 V	Compact local protection	PTVS5VS1UR, PTVS12VS1UR, PTVS24VS1UR
High-Power Front-End DC Bus	380-420 V	Multi-kW surge suppression	SMCJ440A, SMDJ440A class solutions
Rectifier and PFC Stage	400 V bus	5-10 kW surge protection	SMCJ series, SMDJ series (up to 3 kW currently available)
Rack-Level Power Entry	AC mains	High-energy surge protection	SMDJ family with higher-power roadmap devices (5 kW/8 kW under evaluation)

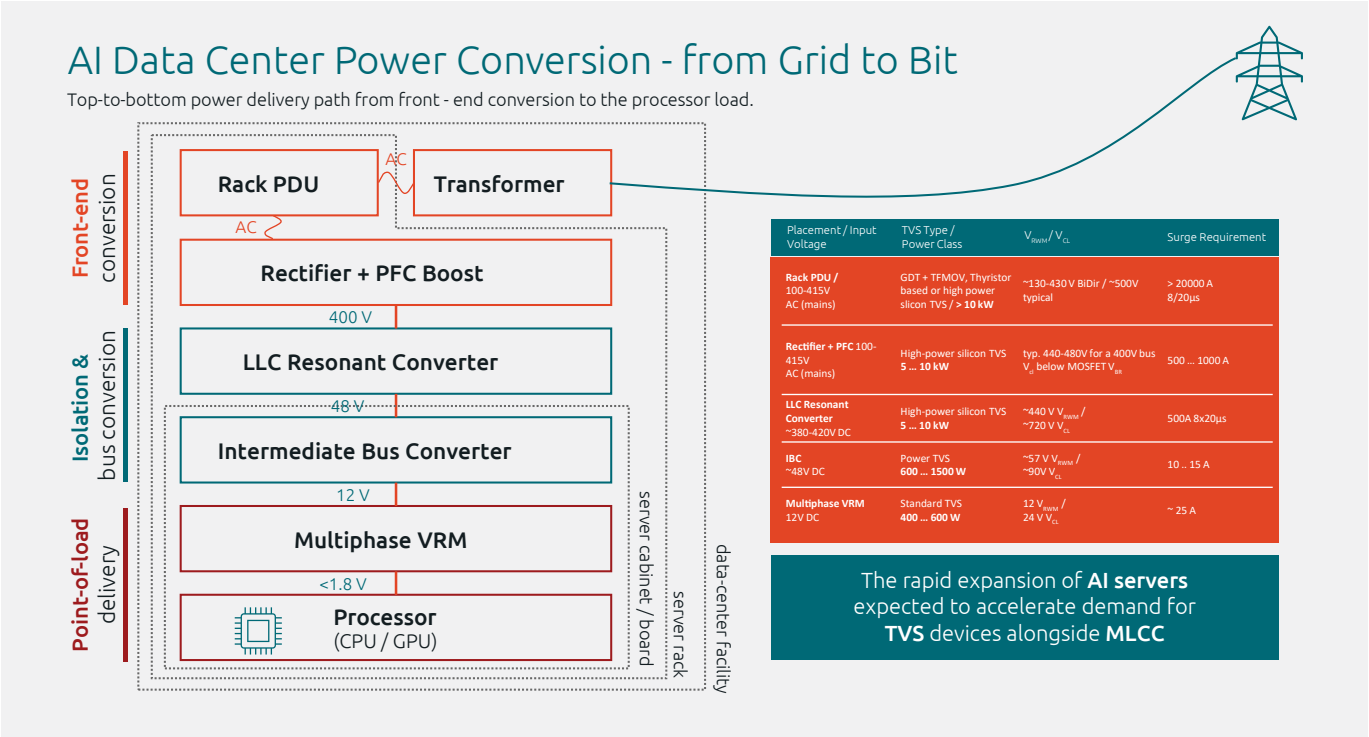


Fig. 33 TVS protection for data center equipment

6. Recommended products

Products	Description	Key part numbers
High power AC/DC conversion – SST and PSU		
Gate drivers	120 V, 4 A peak high-performance dual MOSFET gate driver 28 V, 5 A dual channel non-isolation gate driver	NGD4300, NGD31251
Isolation Transformer Driver	Low-noise, 1.2 A transformer driver for isolated power supplies	NXF6505x, NXF6501x
Digital Isolator	High-Speed, EMC Robust, Reinforced Two-Channel Digital Isolator	NXI772x series
SiC diodes	1200 V, 20 A SiC Schottky diode in TO247 R2P	PSC20120L
1200V SiC MOSFETs	1200 V, 17 and 30 mΩ, N-channel SiC MOSFET	NSF017120L4A0, NSF030120T1A0
750V SiC MOSFETs	750 V, 20 and 40 mΩ, N-channel SiC MOSFET	NSF020750T1B0, NSF040750T1B0, NSF020750L4B0, NSF040750L4B0
650V GaN FETs	80 mΩ in DFN8080 35-70 mΩ (typ.) in TO-247-3/-4, TOLL and TOLT	GAN080-650EBE, GANC035-650TBH, -UTH, -VSH GANC050-650TBH, -UTH, -VSH, -WSH GANC070-650TBH, -UTH, -WSH
Interlock Logic	Logic layer can structurally block gate driver signals from being enabled simultaneously	74HCS08BQ, 74AUP1G57GM
Medium power DC/DC conversion and battery management – UPS and BBU		
650/700V GaN FETs	80-200 mΩ devices in DFN8080, DFN5060 and DPAK packages	GAN080-650EBE, GAN140-650FBE, -EBE GANE190-700BBA
80-200V GaN FETs	1.2-11 mΩ devices in WLCSP, FCLGA, VQFN4x6, PQFN3x5 and PQFN3.3x3.3 packages	GANE0R5-040QTL, GANE0R8-100QTM, GANE1R2-100QTM GANE011-080CBA, GAN7R0-150LBE, GANE1R8-100QBA
Power MOSFETs	40, 60, 80 and-100 V Switching MOSFETs in LFPAK and MLPAK 3x3 and 5x6 for low voltage DC/DC conversion	PSMN1R0-40YLD, PSMN2R6-80YSF, PSMN9R8-100YSF
Power MOSFET	25 V and 100 V Low Rdson MOSFETS in large 5x6, 8x8 and 10x10 packages for Hot-swap and power switch functionality	PSMNR51-25YLH, PSMN2R3-100SSE, PSMN1R0-100ASF
Schottky diodes	Trench Gen2 100 V diodes in CFP2-HP, CFP3-HP, CFP3, CFP5, CFP15 packages with current ratings from 1-20 A	PMEG100Y10ELXD, PMEG100Y20ELXE, PMEG100Y10ELR PMEG100Y50ELP, PMEG100Y100ELPE, PMEG100Y200ELPE
Protection Logic	Logic devices are used for fault aggregation, fault latching and rapid asynchronous response, achieving reaction times as low as 2 ns.	74LVC1G332GW

7. References

Nexperia handbooks and techbooks

MOSFET and GaN FET application handbook
Bipolar Junction Transistor (BJT) Application Handbook
Diode fundamentals, characteristics and applications
Techbook | Power_Input_Protection
Techbook | Power_Management_Techbook

Application Notes

AN50005 | Paralleling power MOSFETs
AN90005 | Understanding power GaN FET data sheet parameters
AN50019 | Thermal boundary condition study on MOSFET packages and PCB substrates
AN90030 | Paralleling of Nexperia cascode GaN FETs in half-bridge topology
AN90041 | Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs
AN90048 | Understanding of critical SiC parameters for efficient and stable designs
AN90067 | X.PAK SiC MOSFETs: A Technical Guide
AN90074 | Comprehensive Benchmarking of 1200V SiC MOSFETs in D2PAK7
AN90081 | How to pick a hot-swap MOSFET

Evaluation/Reference design boards

NEVB-NSF-XPAK-A | 1200 V SiC MOSFET (X.PAK) dual half-bridge evaluation board
NEVB-HB-NSFD7-A | 1200 V SiC MOSFET (TO-263-7) double-pulse half-bridge evaluation board
NEVB-NPS3102A | 12 V, 2-13.5 A, 17 mΩ latching eFuse evaluation board
NEVB-NPS3102B | 12 V, 2-13.5 A, 17 mΩ auto-retry eFuse evaluation board
NEV-DP-GAN039-650NBB | Double pulse evaluation board featuring 33 mΩ GaN FETs in a bottom-side cooled CCPAK1212 package
NX-DP-GAN039-650NTB |650 V GaN FET (top-side cooled) double pulse evaluation board
NX-HB-GAN039-650NTB-TSCUL | 400 V, 3.5 kW GaN FET (top-side cooled) half-bridge evaluation board
NX-HB-GAN039-650NBB-BSCUL | 400 V, 3.5 kW GaN FET (bottom-side cooled) half-bridge evaluation board
NX-HB-GAN111-650WSB | 400 V, 2 kW GaN FET half-bridge evaluation board
NX-HB-GAN041-650WSB | 400 V, 3.5 kW, 100 kHz GaN FET half-bridge evaluation board
GAN039-650NTB | 4 kW, 85-265 Vac analog bridgeless totem-pole PFC evaluation board
Microchip MIC2129 | 48-to-12 V power conversion
Analog Devices EVAL-LTC4286-| 54 V, 36 A Hotswap
Analog Devices EVAL-LTC4287 | 54 V, 72 A Hotswap
TI PMP23496 | 8 kW Hotswap

Other collaterals

Blog | Why all SiC Schottky diodes are not made equal
Blog | 8 Reasons Why Silicon Carbide Diodes Outperform their Silicon Peers
Blog | Discover 4 Advantages of Nexperia's SiC MOSFETs
Brochure | From SiC to thin SiC diodes
Leaflet_| GaNFETs_2026
Video | Switching Performance of Silicon Carbide vs. Silicon Diodes
Video | MPS Silicon Carbide Power Diodes Explained

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