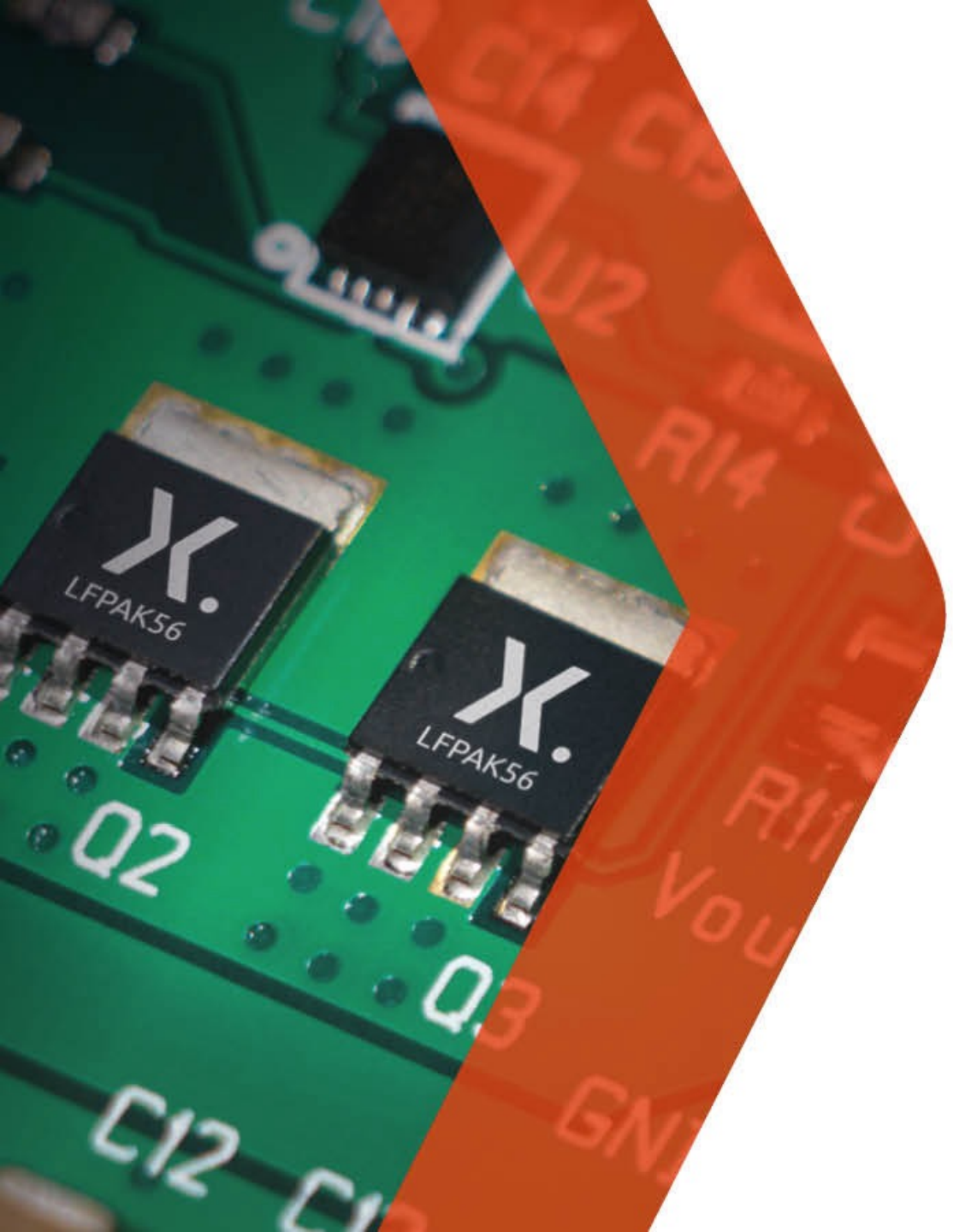

nexperia

Paralleling MOSFETs in high power applications

September 2021

Introduction

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- Principal Applications Engineer

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- International Product Marketing Manager

Contents

- Overview
- MOSFET parameters & influence on dissipation
- Circuit optimization
- PCB Layout influence
- Summary

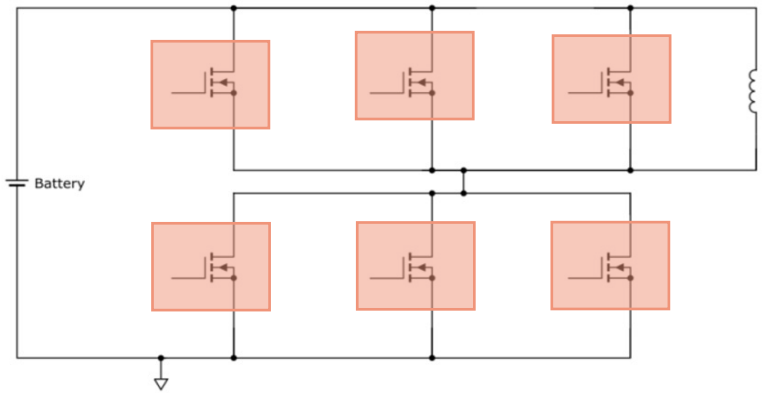
Parallel MOSFET Applications

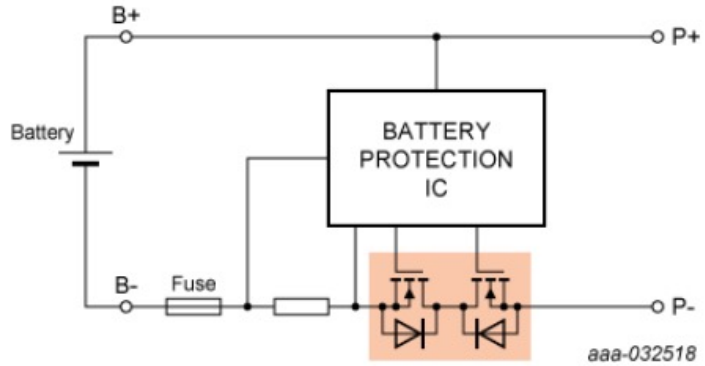
PWM

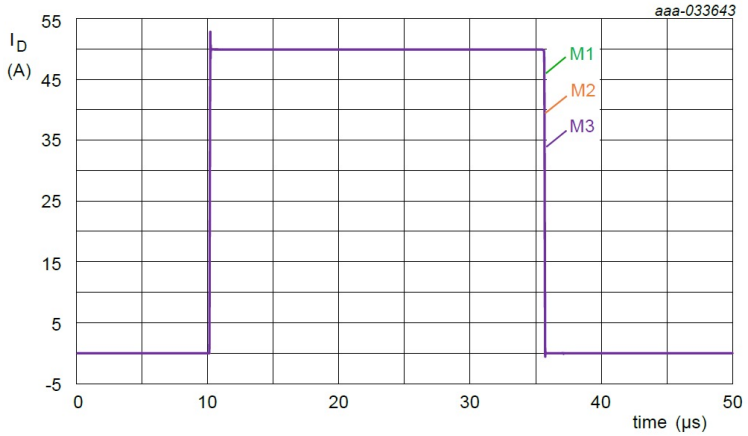
- Motor drive
- Switched mode PSU

Load Switching

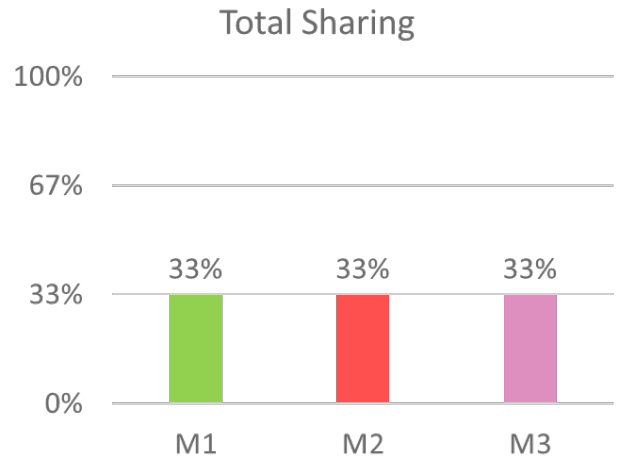
- Safety switch
- E-fuse







IDEAL



MOSFET Parameters

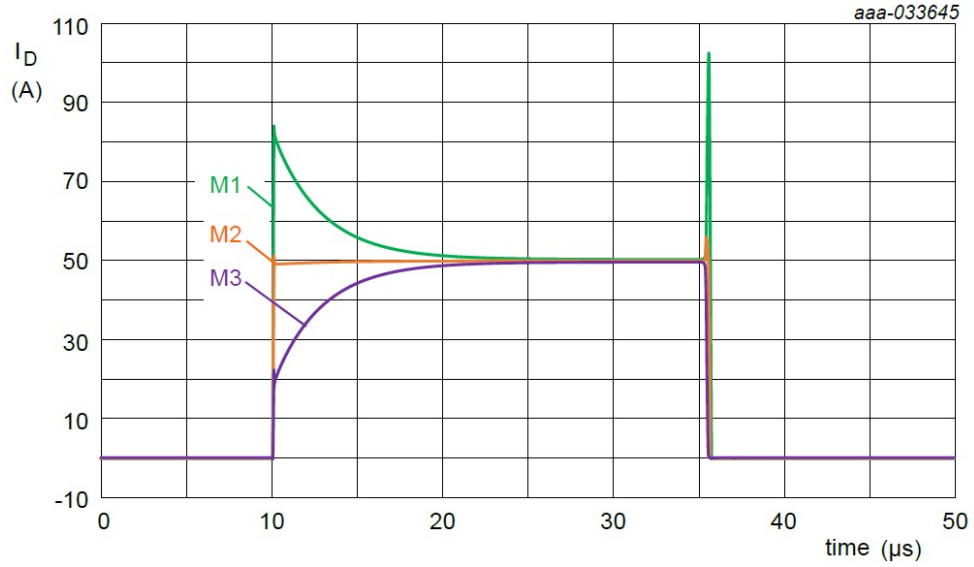
$V_{GS(th)}$ Spread: Current Sharing

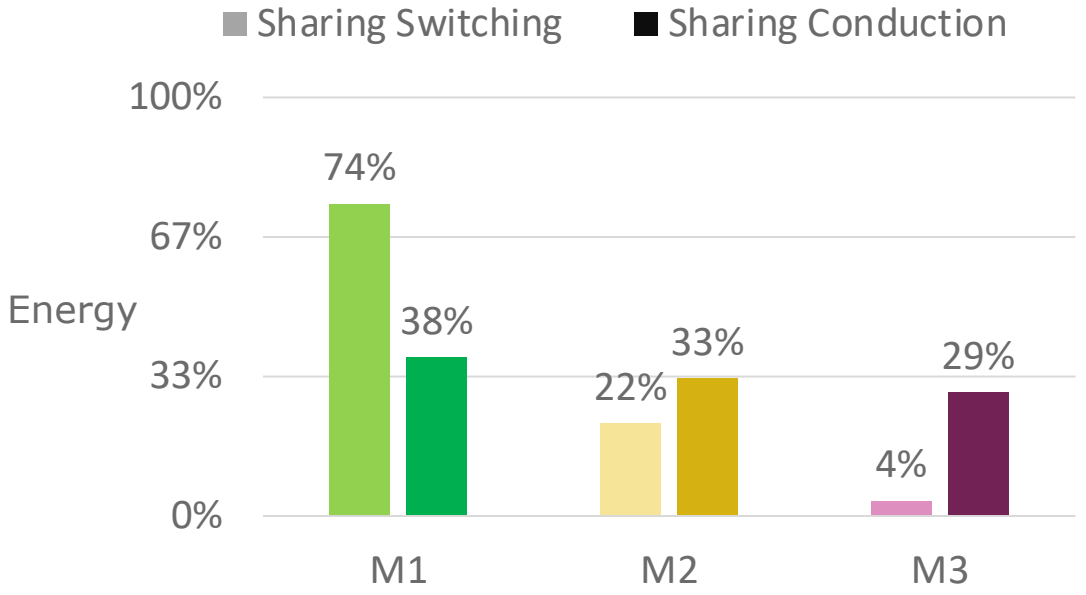
- M1: $V_{GS(th)}$ = 2.4 V
- M2: $V_{GS(th)}$ = 3.0 V
- M3: $V_{GS(th)}$ = 3.6 V

Worst case spread from datasheet

$V_{GS(th)}$ [V]	Conditions
2.4 (min)	V_{DS} = 12 V, I_D = 1 mA
3.0 (typ)	
3.6 (max)	

Latest T9 has improved 1.2 V $V_{gs(th)}$ spread



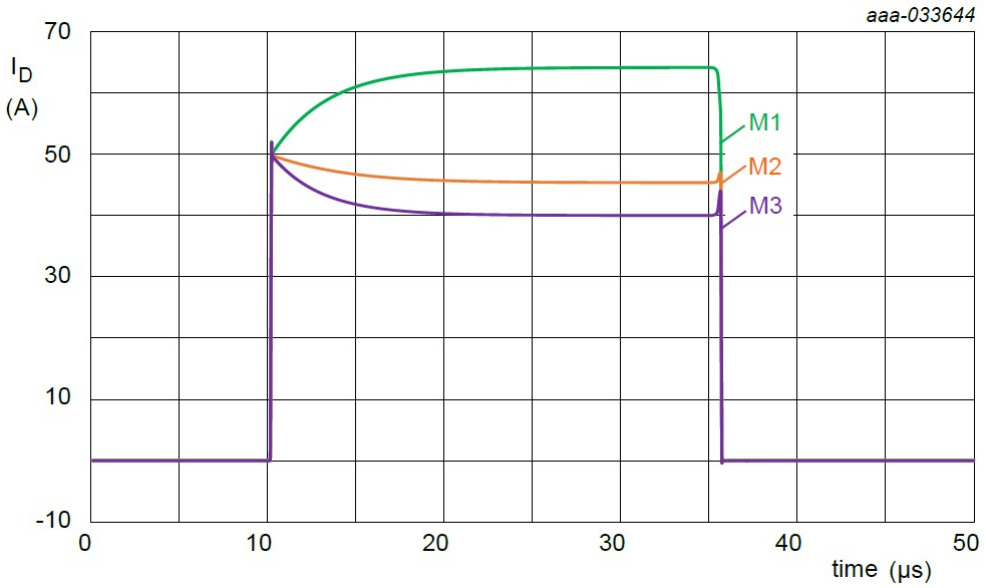


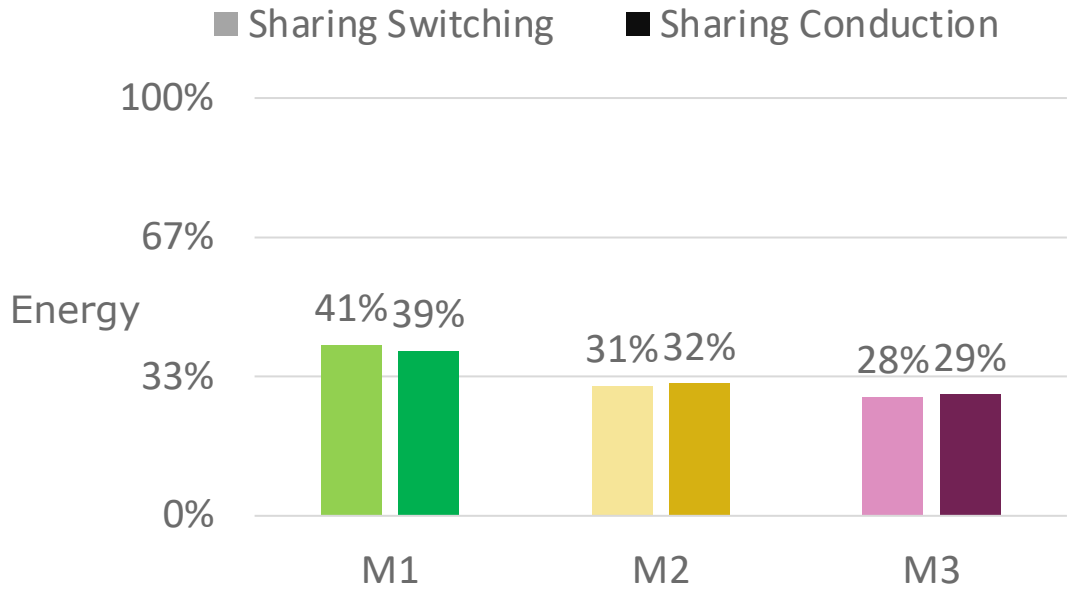
$R_{DS(on)}$ Spread: Current Sharing

- BUK7S1R0-40H
- M1: $R_{DS(on)}$ = 0.62 mΩ
- M2: $R_{DS(on)}$ = 0.88 mΩ
- M3: $R_{DS(on)}$ = 1.00 mΩ

Worst case spread from datasheet

$R_{DS(on)}$ [mΩ]	Conditions
0.62 (min)	V_{GS} = 10 V, I_D = 25 A, T_j = 25 °C
0.88 (typ)	
1.00 (max)	



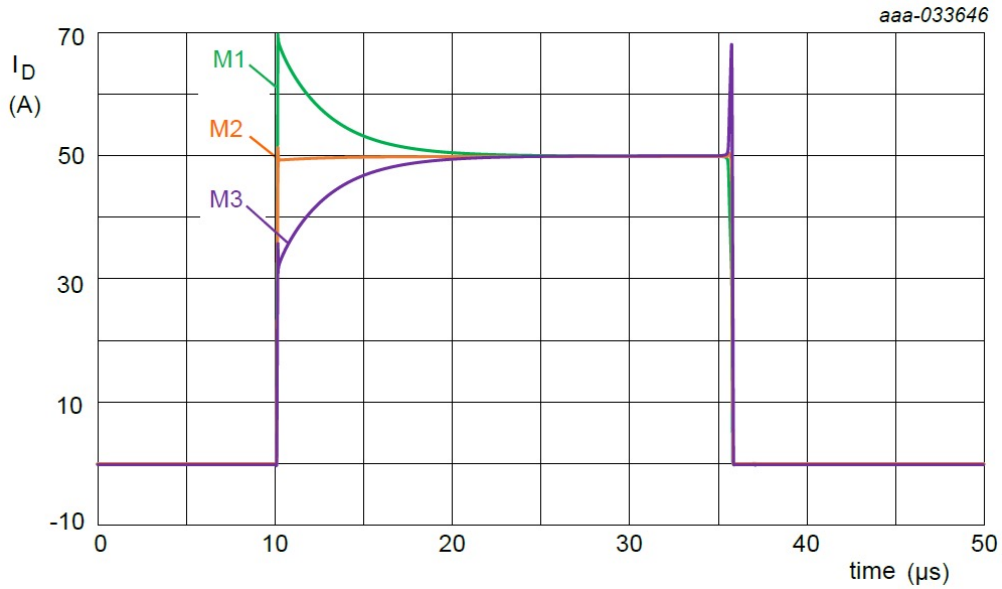


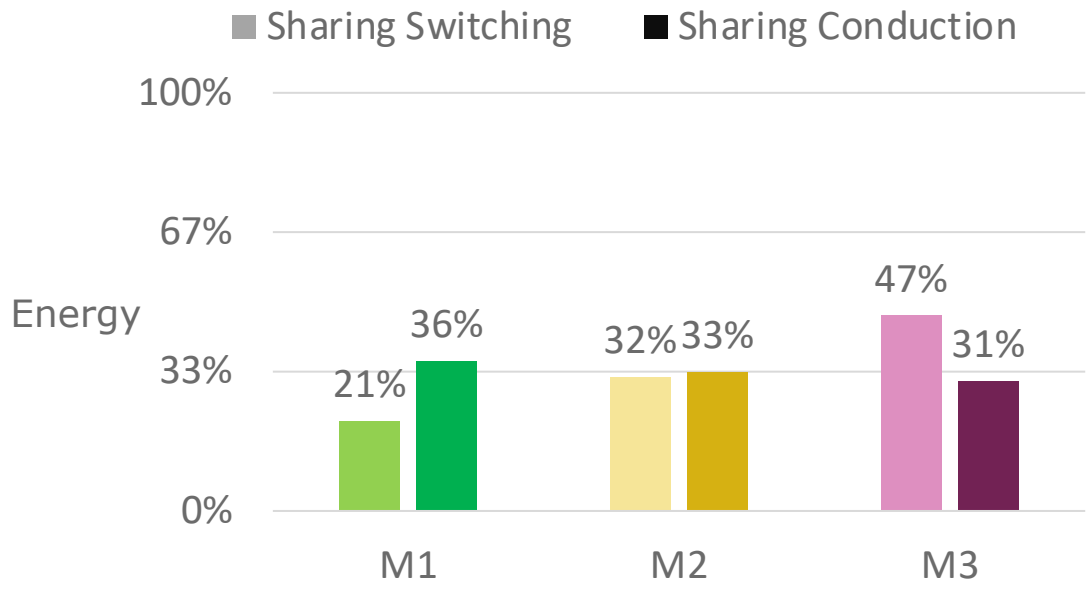
$Q_{G(tot)}$ Spread: Current Sharing

- M1: $Q_{G(tot)}$ = 94.4 nC
- M2: $Q_{G(tot)}$ = 125.7 nC
- M3: $Q_{G(tot)}$ = 158.0 nC

Worst case spread from datasheet

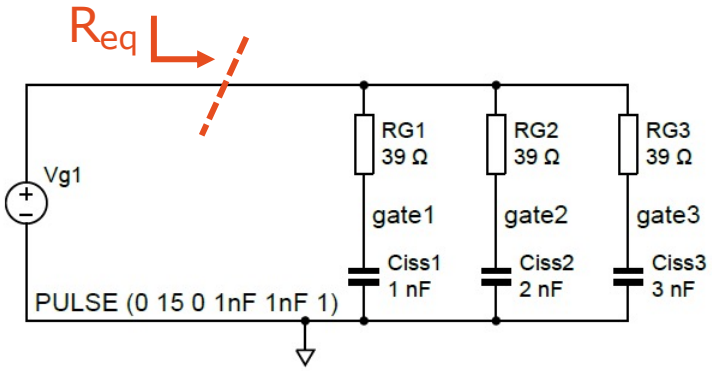
Q_{GS} [nC]	Conditions
27.148	V_{DS} = 32 V, I_D = 25 A, V_{GS} = 10 V
40.024	
Q_{GD} [nC]	
17.008	
34.211	

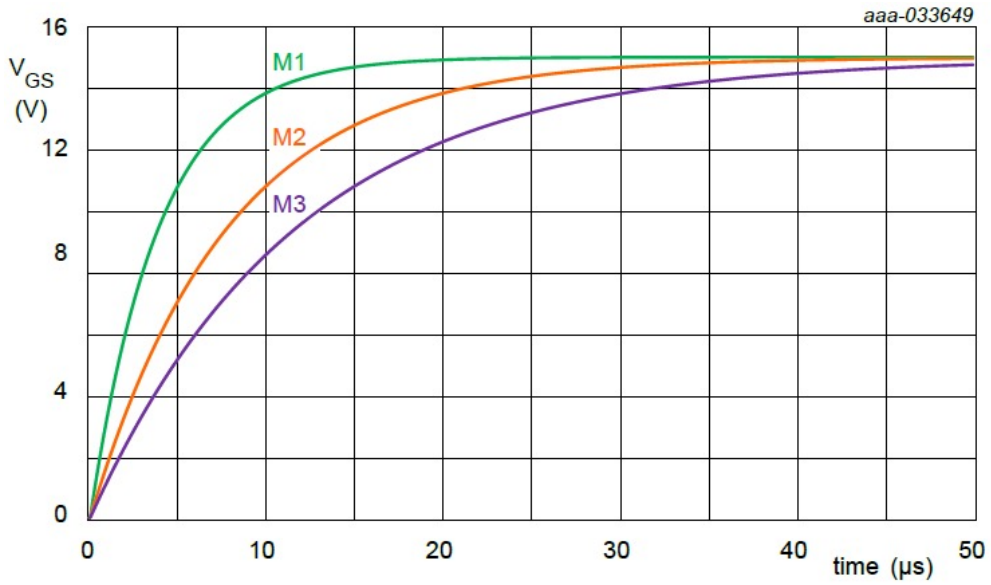


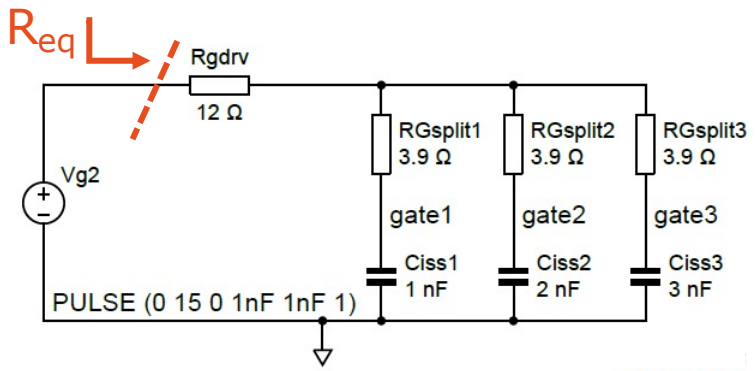


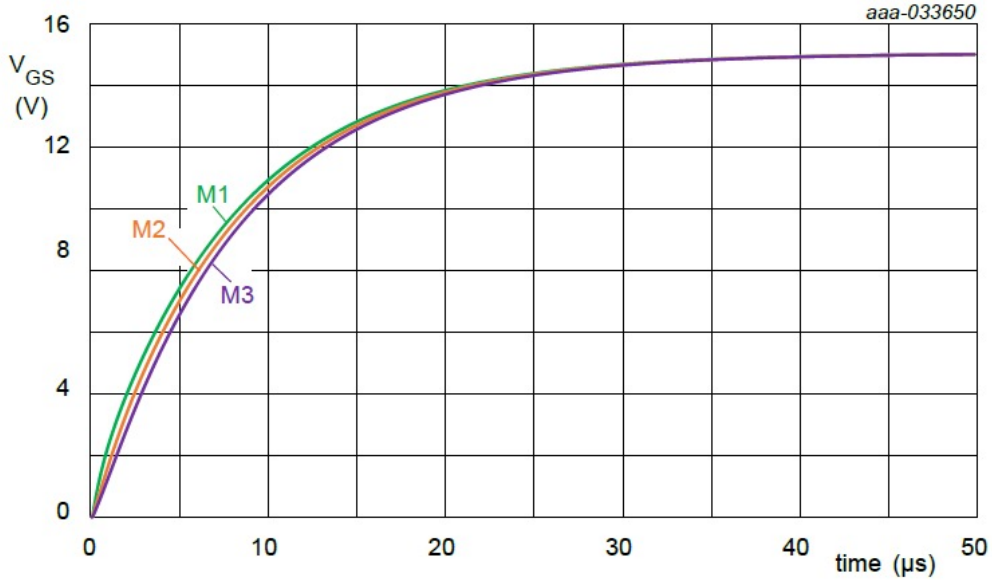
Circuit Optimisation

Localized Gate Resistor Split

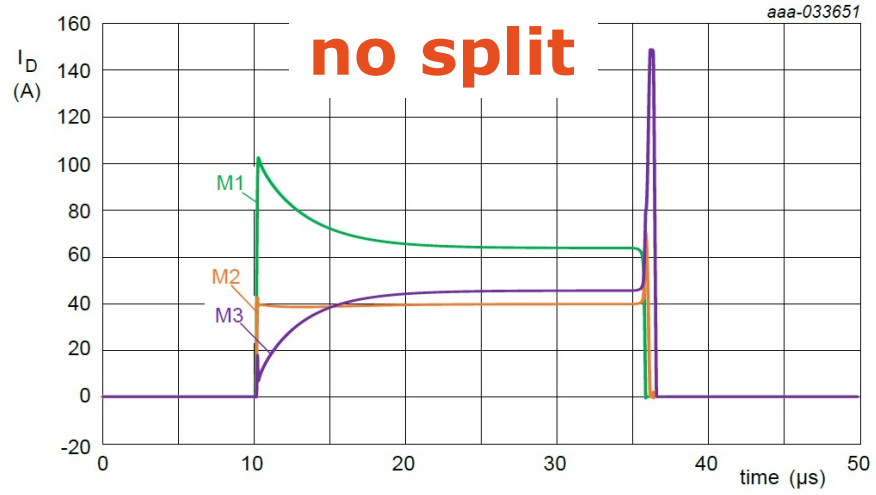


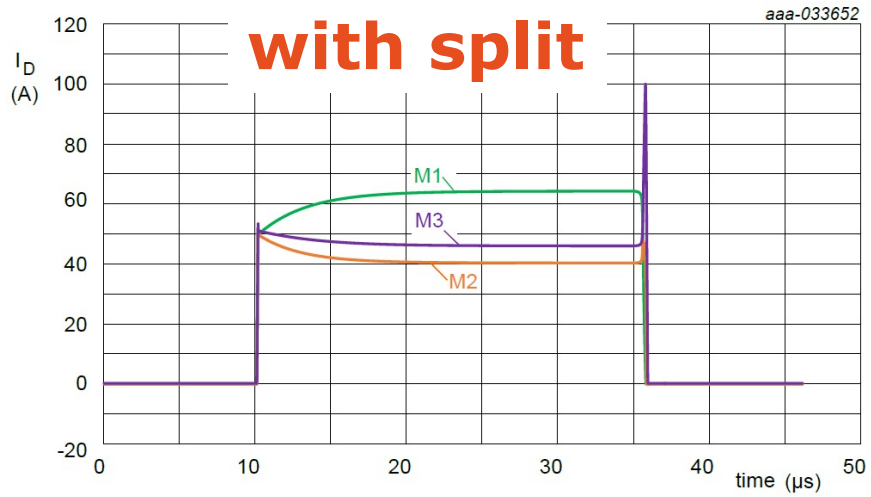


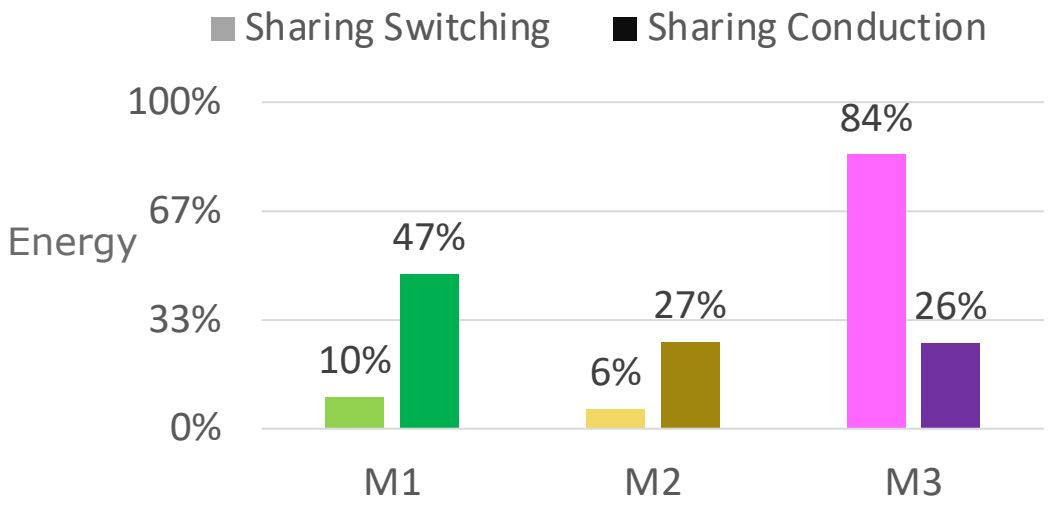


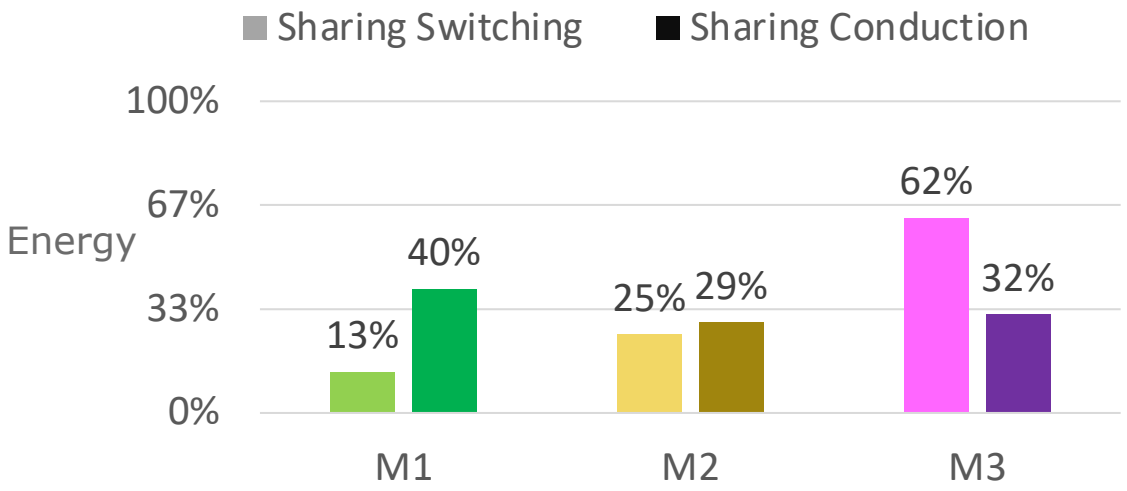


Impact of Gate Resistor Split





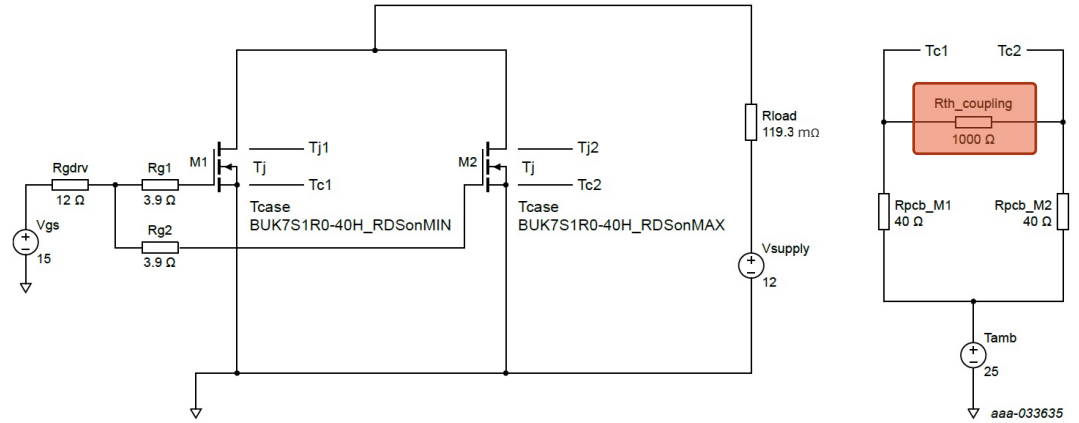


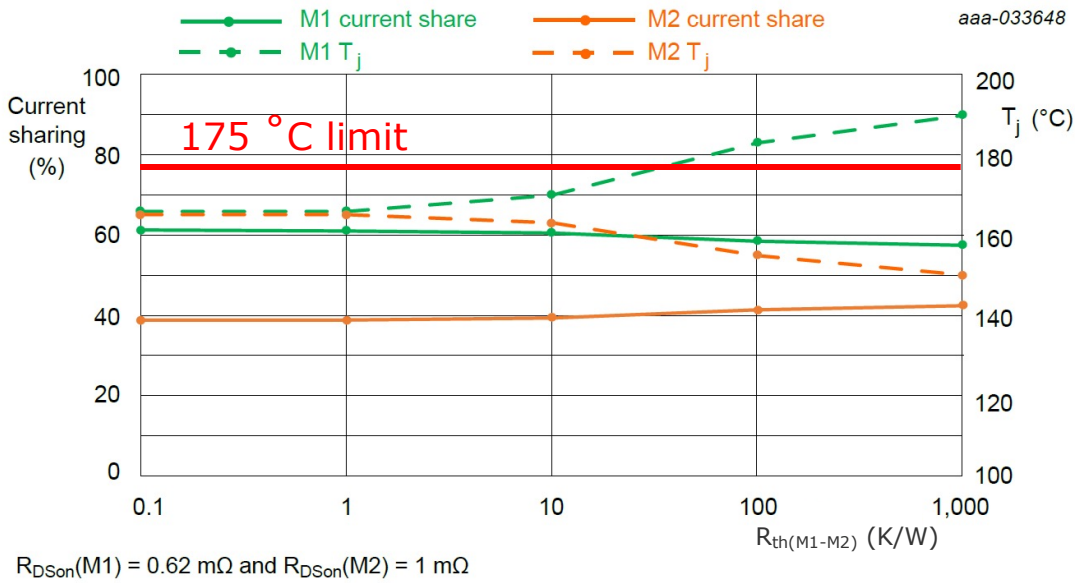


PCB Layout

Temperature Dependency: Thermal Coupling

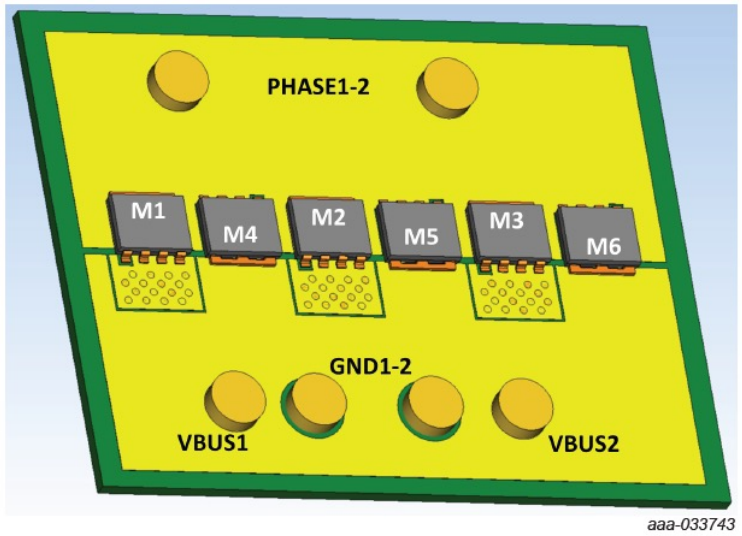
- $R_{DS(on)}$ Positive Temperature Coefficient improves sharing when each paralleled MOSFET is thermally isolated from the others – $R_{th(coupling)}$ is high
- However the junction temperature can easily exceed the 175 °C limit!
- Good thermal coupling between paralleled MOSFETs is preferred as it allows for overall lower T_j

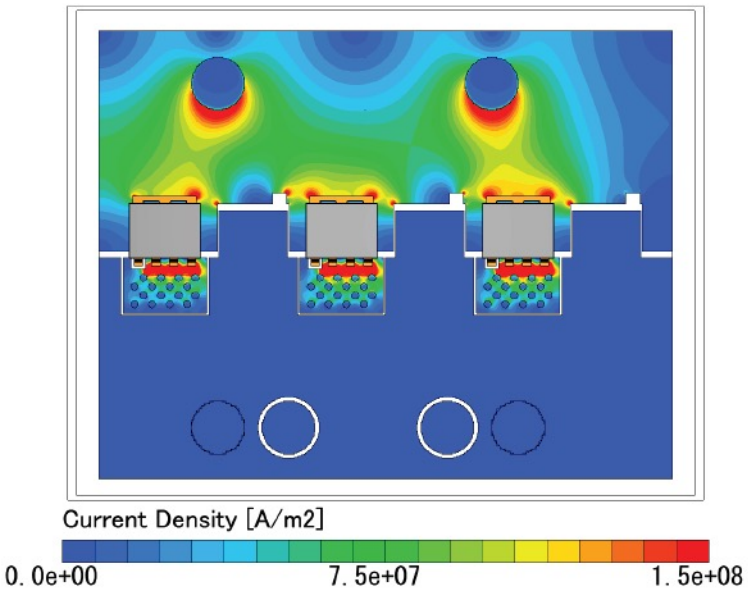


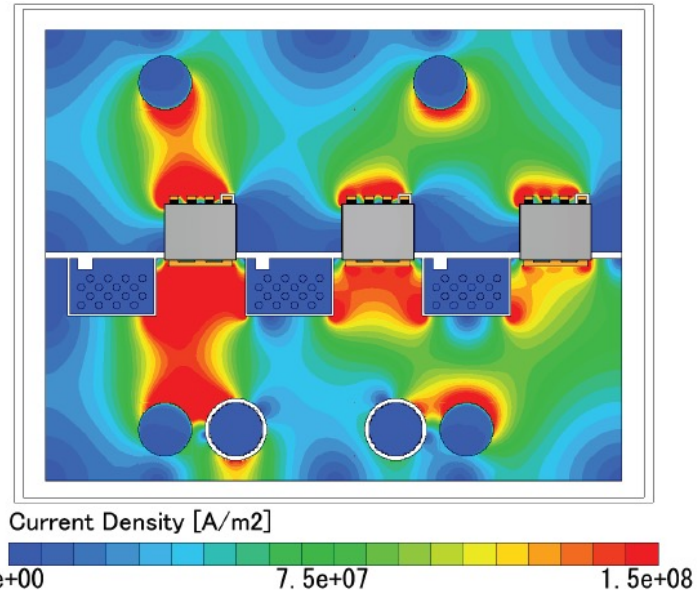


R_{DSon}(M1) = 0.62 mΩ and R_{DSon}(M2) = 1 mΩ

Current Density Simulation







Recommend to use current flow simulation to optimise layout

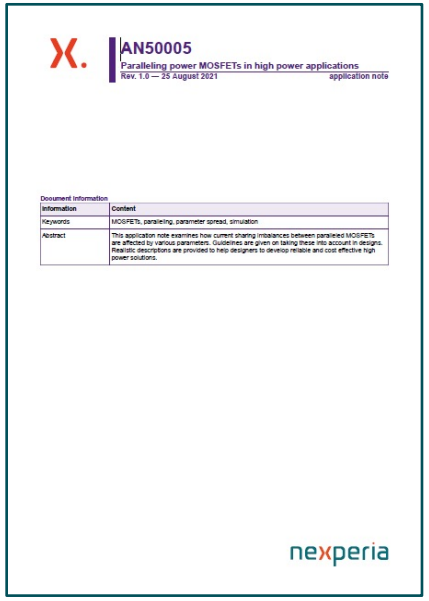
M1 M2 M3
Low Side Active
Good current share due to layout

M4 M5 M6
High Side Active
Current share due to layout could be optimised

*Simulation from scSTREAM by Cradle

Summary

- MOSFET parameters when paralleling: consider V_{th} as the most important, then $R_{DS(on)}$ and finally Q_g has the least influence on behaviour overall.
- Circuit layout should be considered:
  - optimise thermal coupling
  - current path should be balanced – use simulation
- For more detail Nexperia have a new paralleling applications note AN50005 available now
- Interactive Application Note; IAN coming soon
- For more information, please go to www.nexperia.com



Please share your questions and insights

EFFICIENCY WINS.