Automotive

Signal Processing

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Contents

1. Introduction

Every automotive application can be divided into functional blocks in terms of the electronics that they contain. First of all, there are electronic blocks that deal with power and electronic blocks that deal with information. Bot of them have an interface to the surrounding environment and a main hub for processing the information or power.
In this respect the power electronics blocks are:

- Power Input Protection
- Power Management

While the signal electronics blocs are

- Communication Interface
- Signal Processing

These four blocks define a basic automotive Electronic Control Unit (ECU). However, there is no use of having an Automotive ECU without its main functionality. A fift block is therefore necessary in order to provide the means for controlling the main functionality of the application:

- Load Management

Therefore, the Load Management block is specific for every application: LED drivers for lighting units; MOSFET inverters for BLDC drivers; radar transmitters; camera lenses; lasers for lidars; amplifiers for audio and antennas for wireless communications.

The first four blocks are universal for most applications in their nature. However, there might be a difference in their scales. A central computer or ADAS control unit might have a large Signal Processing requirement that would require fast Communication Interface and substantial power requirements for the Power Management and Input Protection blocks. Compared to a lighting module that would still require substantial power but much less signal processing and communication bandwidth.

The interconnections of these blocks within the application of a Zone Control Unit are displayed below in Fig. 1.

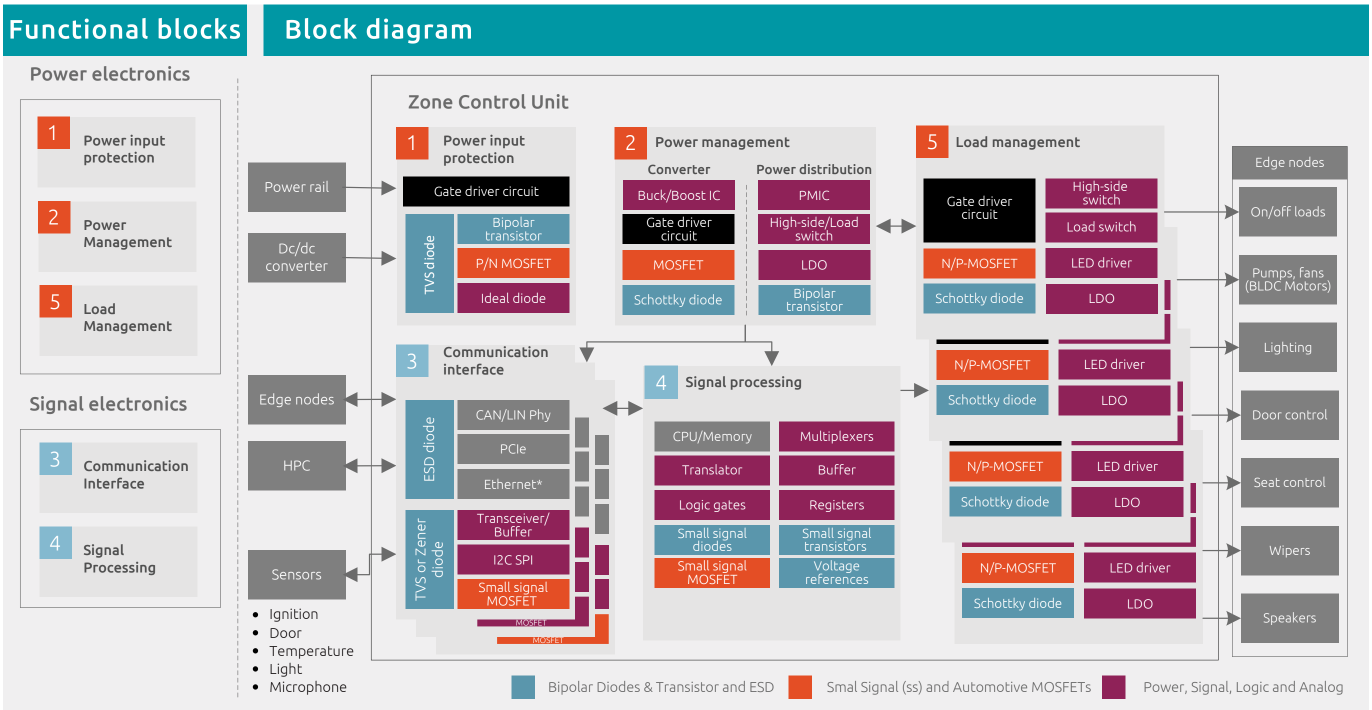


Fig. 1 Zone Control Unit internal electronics block diagram

As the main function is distribution of power and communications to the local actuators, the corresponding blocks appear multiple times.

1 The Power Input Protection block can take up substantial size and large power devices. Besides protecting the rest of the circuit from power surges it can also interconnect various energy supply sources like the batteries and dc/dc converter. It is important to protect the supplies in case the other collapses. It can also appear in several voltage levels like 12 V and 48 V in case the vehicle contains both power nets.

2 The Power Management block contains the means for transforming the incoming voltage to a level that is suitable for the rest of the components. The resulting voltage rails are used to fuel the signal processing and communication blocks. In vehicles with 48 V board nets, this is the place to transform the 48 V to 12 V or 16 V to supply legacy actuators. This is done via high power resonant converters, such as the Switched Tank Converter.

3 The Communication Interface block consists of a variety of communication protocols. Some of these could be analog and slow digital inputs towards sensors. Somewhat faster like IVN and ESD towards information rich peripherals such as ADAS cameras and radars. Audio signals can be transmitted to local speakers and received from microphones. Finally, the received information is translated and packed in a fast Ethernet protocol to communicate with other ZCUs and the central High-performance computer. All these information feeds need to have appropriate protection via ESD or TVS diodes, according to the speed and strength of the signal.

4 Finally, the Signal Processing block contains the Controller and Memory blocks. From the Nexperia arsenal logic gates and registers can be used to establish additional layers of logic and safety that are independent of the main controller; small signal discrete devices can be used for conditioning signals from nearby sensors; and multiplexers and analog switches to increase the digital and analog input channels of the controller.

In this Techbook the Signal Processing block is described in more detail. The challenges a designer might face are addressed with a proposal of appropriate devices and their design in procedures.

2. Design challenges and solutions

The Signal Processing block receives input data from other ECUs and sensors via the Communication interface block and is powered from the Power Management block. It hosts sensitive and central components like processors, SoCs and memory blocks and it does the computations needed to process the input signals and computes the signals needed to control the load via the power components of the Load Management block.

2.1. Interfacing blocks and devices that operate at different voltage levels and have different input and output configurations.

Processor technologies (microcontrollers, SoCs, ASICs, microprocessors) are moving to smaller process geometries and therefore core and I/O voltages are scaling down. As a result there are more I/O level mismatches likely to arise between processors and peripheral devices. Voltage translators are required between process families that are usually connected to 5 V or higher supply (HC(T), AHC(T), VHC(T) and LVC), 3.3 V (LV, LVC, LVT, ALVC, NXT, NXS, NXB, LSF, NXU) and lower supply (AUP, AVC).
Well-tested and proven functional blocks are sometimes used in new designs. These might be on a different voltage or technology than the rest of the design they need to be connected to. Additionally, different function blocks or different logic technologies can be at different logic levels and need interfacing. For complete information on Nexperia Logic devices, refer to the Logic handbook.
There are several possibilities for the input and output solutions that need to be taken into account. The inputs can be:

- Clamp diode protected inputs, enables high to low voltage translations, with an additional current limiting resistor (Fig. 2)
- ESD protected to enable high to low voltage translations (Fig. 3)
- Low threshold inputs, can be used for low to high level translation
- Schmitt trigger inputs, to remove noise from signals (Fig. 4) and improving signal integrity related to slow rising signals in noisy automotive environments. Nexperia has a wide voltage range of devices available from below 1 V to 5.5 V.

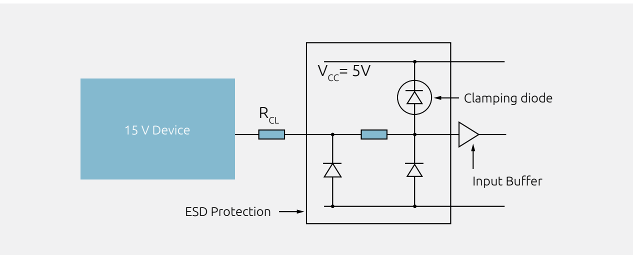


Fig. 2 Clamp diode protected input simplified schematic

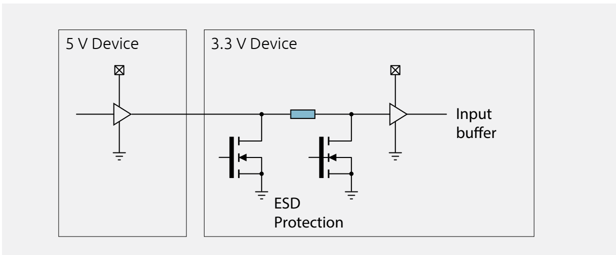


Fig. 3 ESD protected inputs simplified schematics

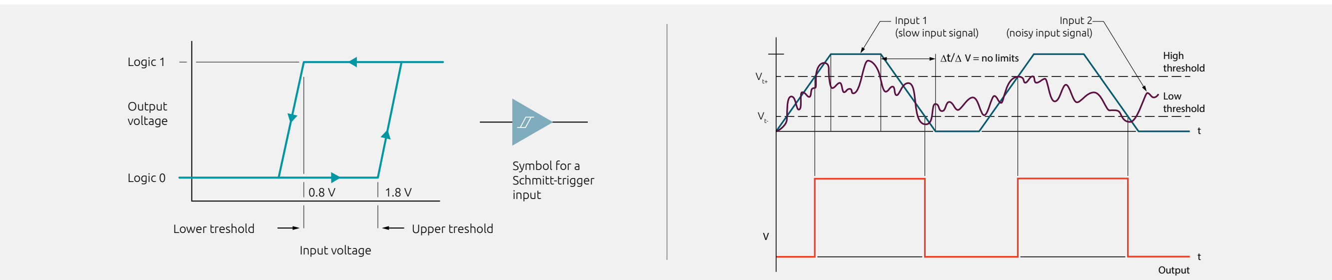


Fig. 4 Schmitt trigger inputs hysteresis curve (left) and signal response (right)

While device outputs can be:

- Open drain outputs, enables low to high and high to low level translations (Fig. 5)
- I_{off} restricted outputs, enables lower consumption in application power-down mode
- Impedance matched to the load to prevent signal ringing in circuits with longer wiring
- Bus hold outputs: prevents floating inputs to CMOS circuits from stalling at $V_{CC}/2$ and causing shoot-through current. A weak feedback mechanism to the input pin ensures the last applied state is held at the input (Fig. 6).

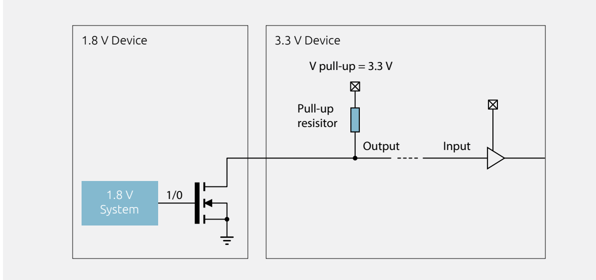


Fig. 5 Open drain outputs simplified schematic and example of utilisation.

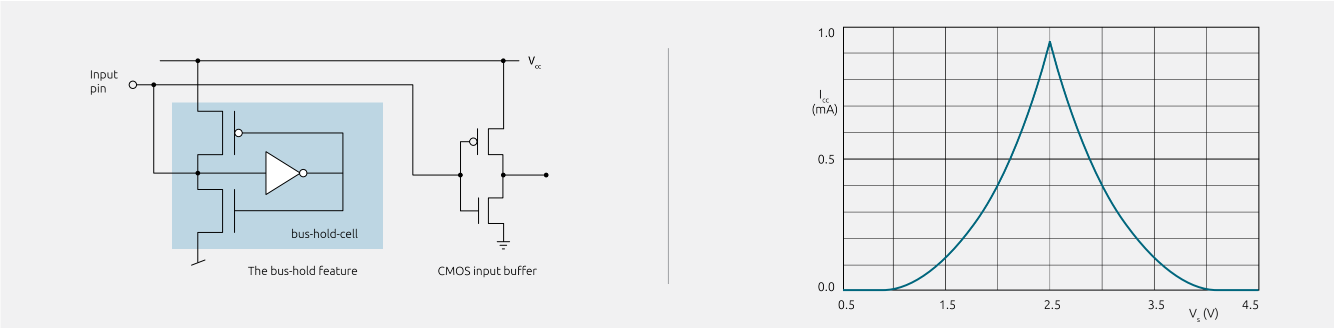


Fig. 6 Bus hold feedback functional schematic (left) and output current and voltage graph (right).

A feature of many buffers and translators is to prevent current through the device body diode when the system is partially powered down. In this way the particular device pin is protected from potentially large currents and the powered down system cannot malfunction because of partially elevated V_{CC1}. This feature is better known as I_{off} protection. See illustration in Fig. 33. Partial power down is key for power management, especially important in EV/HEVs.

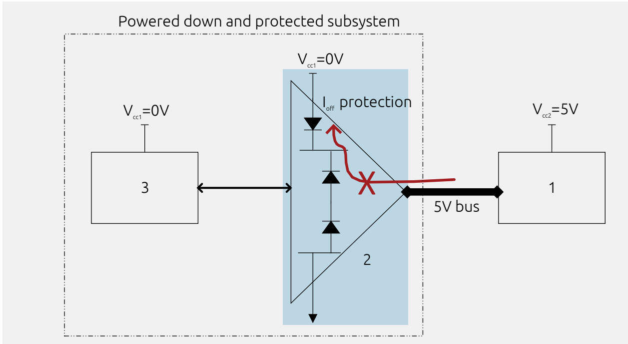


Fig. 7 Device with I_{off} protection

Interface logic is also used to increase low-drive microcontroller outputs to drive high-load peripherals. New processor I/O have limited drive strength because of low core voltage operating modes. Buffers and level translators with good drive strength supplement drive strength of processors I/O to overcome trace or cable capacitance to maintain signal quality.

Except for the voltage level of the circuits they connect, when choosing a translator, there are a number of other factors to be considered, such as speed, current drive strength, topology, and package requirements. The maximum allowed voltage level still allows the translator to operate at lower voltage levels. The newer and faster families have a lower max voltage and less current drive strength.

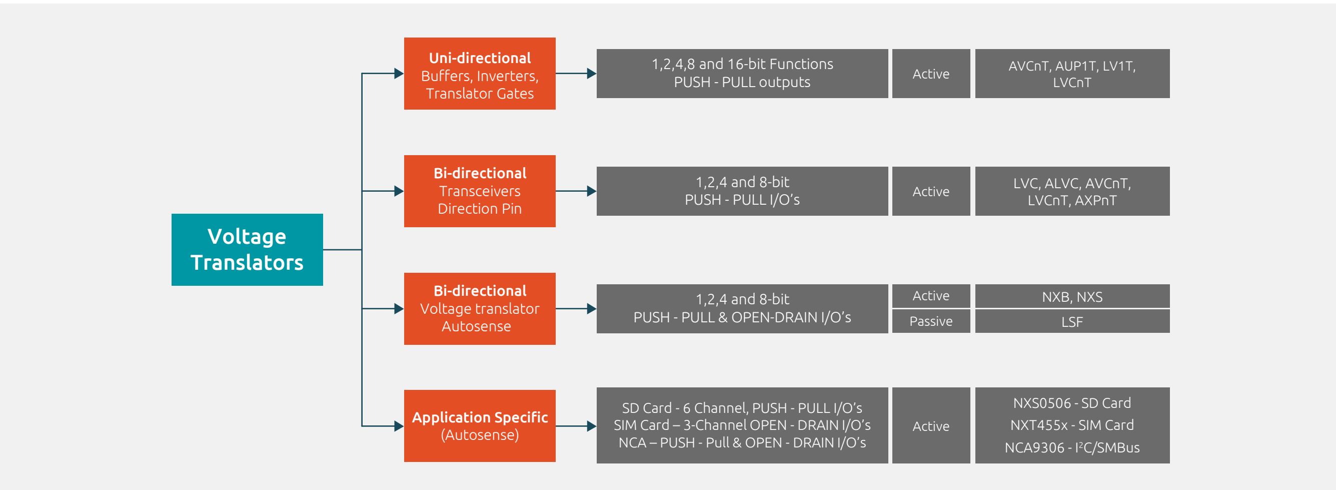


Fig. 8 Voltage translator selector tool: high level summary.

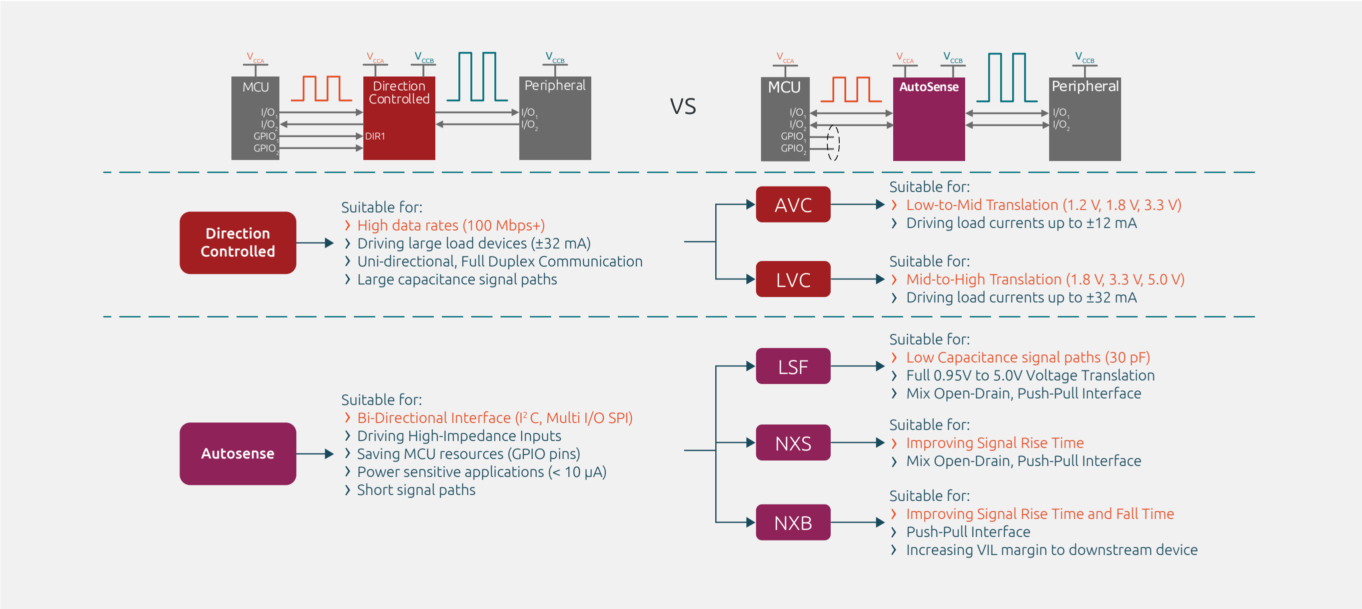


Fig. 9 Bidirectional voltage translator selector tool: Direction Controlled vs. Autosense Voltage Translators.

Use cases that need higher data rates and higher current drive can be addressed by the advanced high-speed CMOS (AVC) and Low Voltage CMOS (LVC) series direction-controlled translators, while the NXU family is intended for fixed direction use cases.

On Fig. 10, an application example for a Connectivity Extension Module in vehicles which need voltage translation supporting RGMII requirements. RGMII with voltage translation is important in applications like vehicle control units, where high-speed and reliable Ethernet communication is needed between the MAC and PHY in a mixed-voltage environment. The NXV family devices have wide dual supply voltage range from 0.9 V to 3.6 V, high output drive (12 mA) and glitch free power supply sequencing.

Level translation devices provide optimal solutions of overcoming I/O level mismatch without sacrificing performance. They are available to address most common logic levels and interface standards such as I2C, SPI, UART, JTAG.

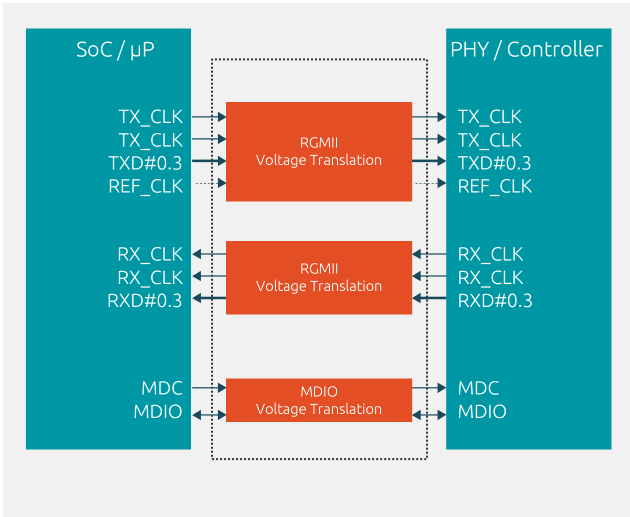


Fig. 10 NXV translator application example between SoC and PHY supporting RMGII requirements.

Level shifting can also be realised with discrete MOSFETs. Application note AN10441 details a bidirectional solution depicted on Fig. 11. In spite of its surprising simplicity, such a solution not only fulfils the requirement of bidirectional level shifting without a direction control signal, it also:

- Isolates a powered-down bus section from the rest of the bus system
- Protects the ‘lower voltage’ side against high voltage spikes from the ‘higher-voltage’ side

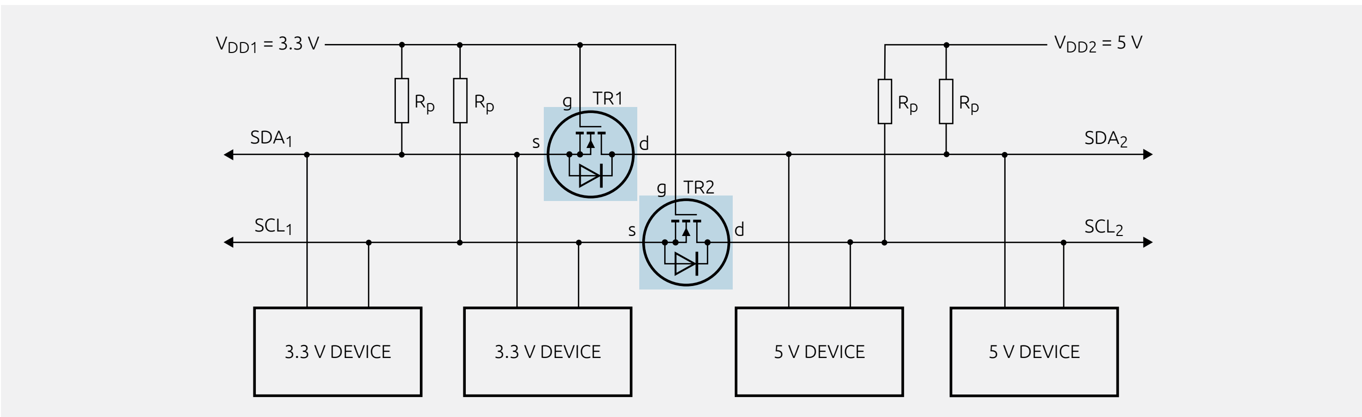
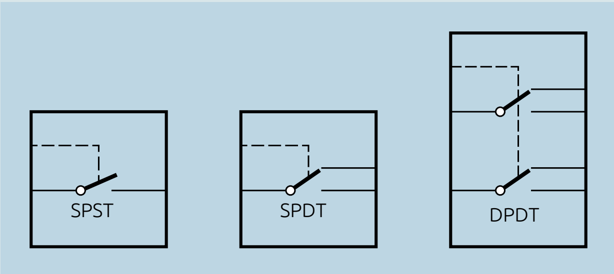


Fig. 11 Bidirectional level shifter circuit connecting two different voltage sections in an I2C-bus system

2.2. Increasing the number of pins of the controller without upgrading the controller.

The increasing number of functions the main controller needs to manage might require more pins than what the controller has. Analog switches and multiplexers can be used to expand the MCU pin count and direct multiple digital or analog input signals to ADC or digital input pins. Various configurations are possible as seen in the figure below. An example product family would be the NMUX130xxx-Q100 1.8 V general purpose SP8T-Z and 2xSP4T-Z analog switches with injection current control:

Suggested Nexperia analog switches: NMUX130-Q100



- Injection current control: Typical coupling of 30 μV/mA
- 1.8 V control logic thresholds across supply operating range
- Complete Powered off protection (V_{CC} = 0 V)
- Isolates biased digital/analog pins from back-powering V_{CC}
- Maintains Hi-Z state of analog switch
- 1.5 V to 5.5 V operating range
- Rail-to-rail operation of analog signal pins
- Pin compatible with legacy 405x/485x analog switches
- ESD protection: ±2 kV HBM and ±750 V CDM
- Specified from -40 °C to 85 °C and -40 °C to 125 °C

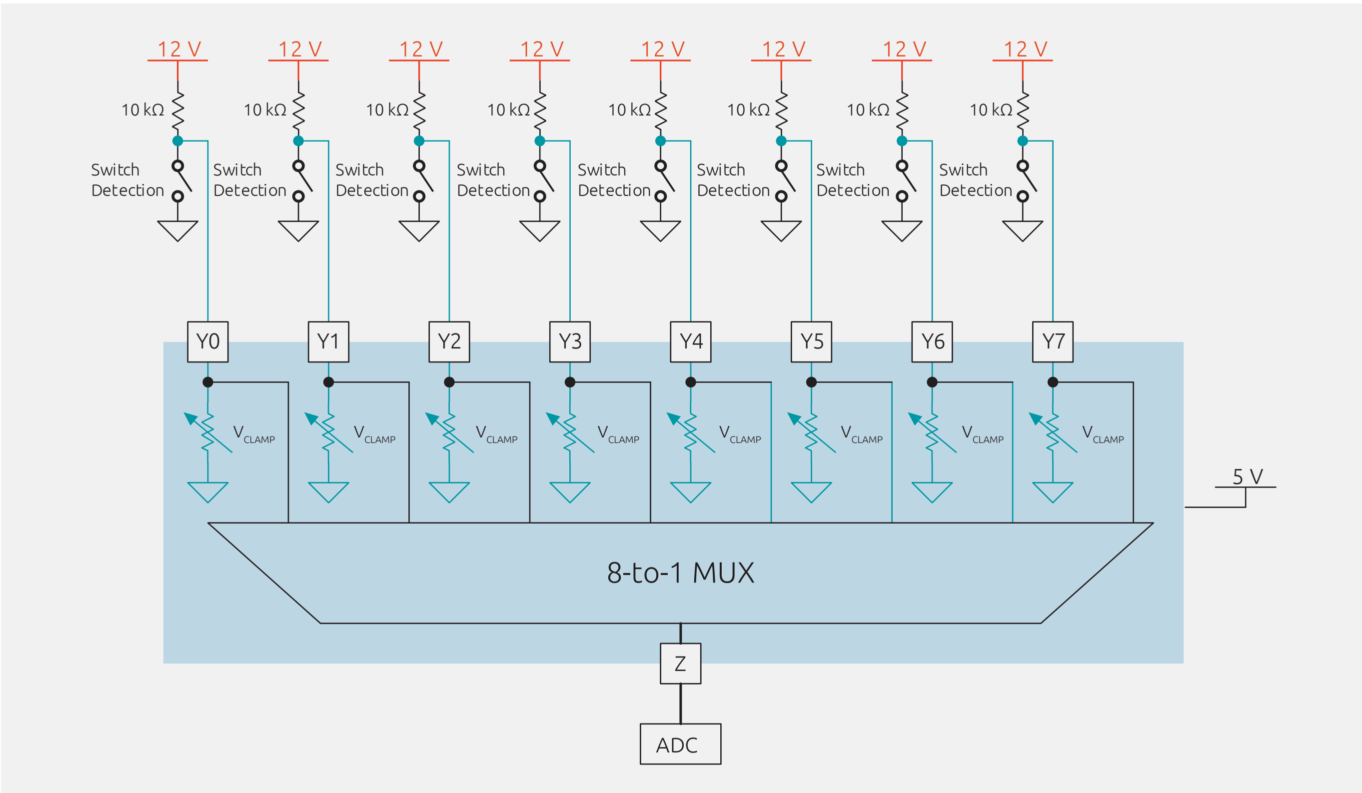


Fig. 12 NMUX130x application example

An example of the application of the NMUX130x is shown in Fig. 12. It can be noted that the analog input is tied to 12 V, but analog supply operates at 5 V. A traditional analog switch would be permanently damaged if the 12V rail reached the analog inputs. But the injection current control feature in NMUX130x clamps the analog input to a safe voltage (V_{CLAMP} ~ 5.5 V). Automotive designs intentionally drive above V_{CC} to create a wetting current that prevents PCB and relay oxidation. Wetting current requires the Injection Current Control feature in NMUX1308. The NMUX1308 also has Input Voltage clamp functionality that prevents saturation of the output in case an inactive input is connected to a high voltage rail. This is illustrated in Fig. 13.

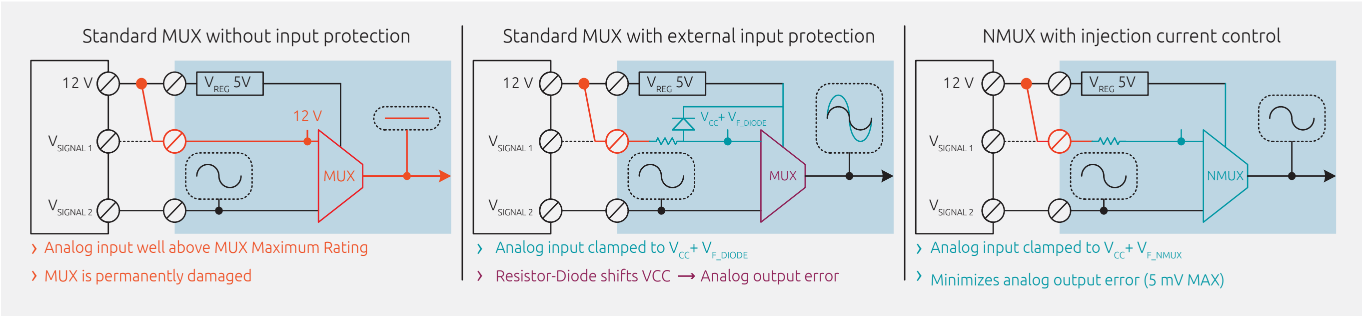
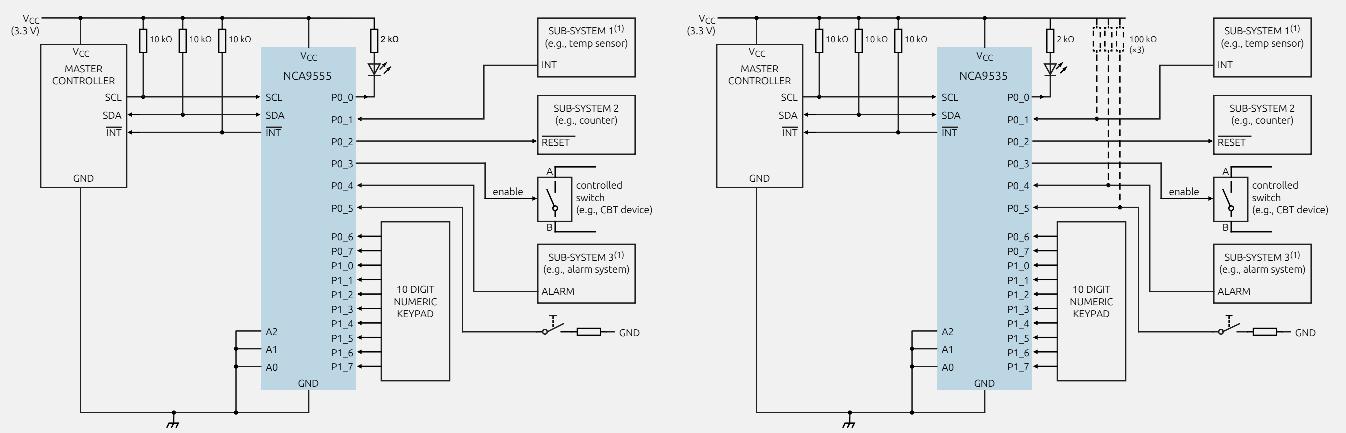


Fig. 13 NMUX130x application example

A good solution to extending the GPIO inputs of the main controller is Nexperia's I2C GPIO extender. The pros and cons of the NCA9555, NCA9535 and NCA9595 are shown in Fig 14.



NCA9555: Internal pull-up resistors present on all IOs

- Advantage: Default state is guaranteed using pull-ups
- Disadvantage: High power during low state

NCA9535: No internal pull-up resistors present on all IOs

- Advantage: Low power; no internal pull-ups
- Disadvantage: Customer need to use external pull up resistors; Extra BOM cost

Fig. 14 I2C GPIO extenders in application circuits

Some of the features of the Nexperia's I2C expanders are:

- Single supply GPIO expander supporting 1.65 V to 5.5 V operation
- Serial to parallel (SDA to P0-P16) and parallel to serial (P0-P16) conversion with I2C protocol
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
- Low power consumption 2.5 μA max
- 400 kHz operation (FM I2C mode)
- Glitch free Power up with all channels configured as inputs with Pull-ups
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Open-drain active LOW interrupt output (INT)
- Configuration pull-up registers to disable pull up resistors on GPIOs
- Noise filters on SCL and SDA inputs
- Overvoltage tolerant inputs to 5 V

2.3. Realize safety, functionality and security features independently from the main controller

Logic circuits, registers, analog switches and voltage translators can be used for added functionality or additional layers of security outside of the main control processor. Because of the large number of process families available, the below table is provided to ease selection, with explanation of what families have which features from the ones listed in Fig. 2 to Fig. 7:

		LV	LVC	LVT	ALVC	CBTLV(D)	AUP	AVC	AXPnT	CB3Q	AUP1T	XS3A	NXT
Parameters	Supply voltage (V)	1.0 - 3.6	1.2 - 3.6	2.7 - 3.6	1.2 - 3.6	1.0 - 3.6	0.8 - 3.6	1.2 - 3.6	0.9 - 5.5	2.3 - 3.6	2.3 - 3.6	1.4 - 4.3	1.1 - 3.3
	Propagation Delay (Typ) (ns)	9	4	2	2	0.15	3.4	1	8	0.2	4	22	7 - 15
	Output drive (mA)	+8	+24	-32, +64	+24	N/A	+1.9	+8	+12	N/A	±4	N/A	
	Standby Current (µA)	20	20	120	40	10	0.9	20	4..13	400	1.4 - 3.5	0.7	
	Maximum Frequency (MHz)	100	280	150	425	400	400	350		20		40	2.5
	AEC-Q100 Grade	Level 1	Level 1	Level 3	Level 1, 3	Level 1	Level 1	Level 1	Level 1	Level 3	Level 1	Level 1	√
Features	Overvoltage Tolerant I/Os		√	√	√	√	√	√	√	√	√		
	Schmitt Trigger Inputs	√	√	√	√			√		√	√		
	Low Threshold Inputs	√						√	√	√	√	√	
	Input Clamp Diodes	√									√		
	Bus Hold		√	√	√		√						
	Power-Off Leakage Protection		√	√		√	√	√	√	√	√		
	Source Termination		√	√	√		√						
	Open-Drain Outputs	√	√					√		√			√
	Low Delay Isolation					√						√	

Table I Nexperia Logic circuits, Registers, Analog Switches and Voltage Translators Overview – Low voltage families

		HEF4000B	HC(T)	AHC(T)	VHC(T)	LV-A(T)	CBT(D)	LVC	LV1T	NXS(B)	LSF	NXU
Parameters	Supply voltage (V)	3.0-15.0	2-6	2-5.5	2-5.5	2-5.5	4.5-5.5	1.65-5.5	1.6-5.5	1.65-3.6 2.3-5.5	0.95-5	0.9 - 5.5V
	Propagation Delay (Typ) (ns)	90	9	5	4	3.4	0.25	1.7	13.5	5.2	0.7	4.5
	Output drive (mA)	±3	±8	±8	±8	±12	N/A	±24	±8	-1 / ±0.02	64	±12
	Standby Current (µA)	600	80	40	40	20	3	10	10	30 .. 70	N/A	5
	Maximum Frequency (MHz)	45	59	110	110	115	300	200		55		125
	AEC-Q100 Grade	Level 1, 3	Level 1	Level 1	Level 1	Level 1	Level 1	Level 1	Level 1	Level 1	Level 1	Level 1
Features	Overvoltage Tolerant I/Os		√	√	√		√	√	√	√	√	√
	Schmitt Trigger Inputs	√	√	√	√			√	√			√
	Low Threshold Inputs		√	√	√				√			
	TTL Inputs		√	√	√		√		√			
	Input Clamp Diodes	√	√									
	Power-Off Leakage Protection							√	√	√	√	√
	Open Drain Outputs		√	√				√	√	√ / -	√	
	Low Delay Isolation						√					

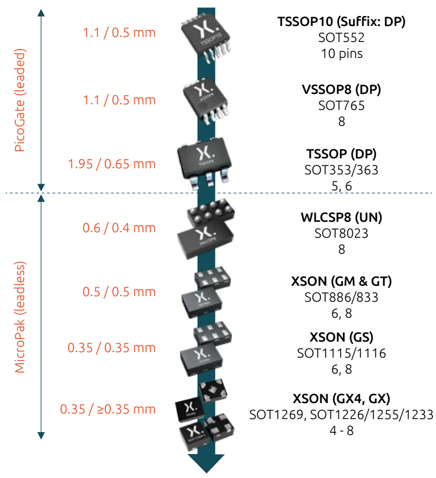
Table II Nexperia Logic circuits, Registers, Analog Switches and Voltage Translators Overview – High voltage families

Category versus Family	ABT	AHC(T)	ALVC	ALVT	AUP	AVC	AXP	CB3Q	CBT(D)	CBTLV(D)	HC(T)	HEF4000B	LSF	LV	LVC	LVT	NCA	NXS / NXB /	XS3A / XS5A /	NMUX
Analog Switches		√									√	√		√	√				√	√
Buffers/Inverters/Drivers	√	√	√	√	√	√		√		√	√	√		√	√	√				
Bus Switches								√	√	√										
Combination Logic					√										√					
Counters/Frequency Dividers		√									√	√		√	√					
Decoders/Demultiplexers		√			√						√	√		√	√					
Digital Comparators											√									
Digital Multiplexer		√			√						√				√					
Flip-Flops	√	√	√	√	√						√	√		√	√	√				
Gates	√	√	√		√						√	√		√	√	√				
Latches/Registered Drivers		√	√	√	√						√	√			√	√				
Level Shifters / Voltage translators			√		√	√	√					√	√	√	√		√	√		
Multivibrators		√									√	√		√	√					
Phase Locked Loops											√	√								
Schmitt Triggers		√	√		√						√	√		√	√	√				
Shift Registers		√									√	√		√	√					
Transceivers	√	√	√	√							√			√	√	√				
# of Family Functions:	15	122	40	9	95	24	4	2	8	14	259	64	4	51	136	37	1	10	7	4

Table III Nexperia logic devices availability in different technologies

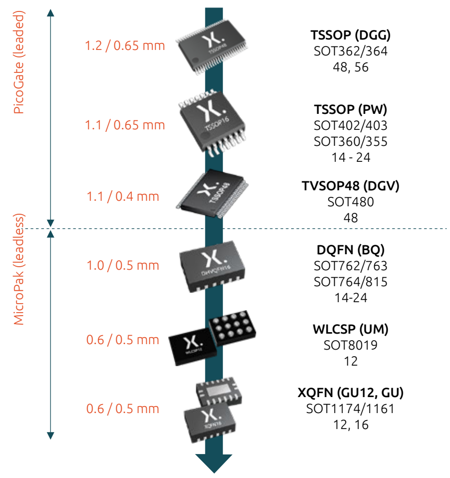
Portfolio	Pin count	Leaded (PicoGate)			Leadless (MicroPak)		
		Suffix	Name	Version	Suffix	Name	Version
Mini Logic (≤10pins)	4				GX4	X2SON4	SOT1269
	5	GW	TSSOP5	SOT353	GX	X2SON5	SOT1226
	6	GW	TSSOP6	SOT363	GX GS GM	X2SON6 XSON6 XSON6	SOT1255 SOT1202 SOT886
	8	DC	VSSOP8	SOT765	GX GS GT	X2SON8 XSON8 XSON8	SOT1233 SOT1203 SOT833
	10	DP	TSSOP10	SOT552	GU	XQFN10	SOT1160

Table IV Nexperia mini logic package portfolio



Portfolio	Pin count	Leaded			Leadless		
		Suffix	Name	Version	Suffix	Name	Version
Standard Logic (>10pins)	12				GU	XQFN12	SOT1174
	14	PW	TSSOP14	SOT402	BQ	DHVQFN14	SOT762
	16	PW	TSSOP16	SOT403	BQ	DHVQFN16	SOT763
	20	PW	TSSOP20	SOT360	BQ	DHVQFN20	SOT764
	24	PW	TSSOP24	SOT355	BQ	DHVQFN24	SOT815
	48	DGG DGV	TSSOP48 TVSOP48	SOT362 SOT480			

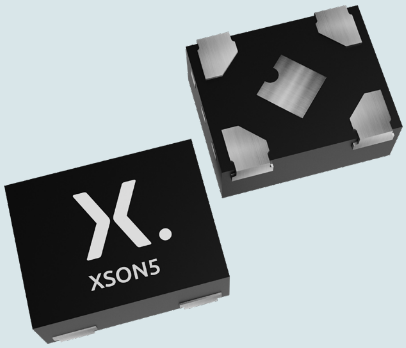
Table V Nexperia standard logic package portfolio



For the increased space constrains Nexperia's MicroPak (XSON5, SOT8065) devices offer solutions. It is the World's first 5-pin mini logic package with Side Wettable Flanks. These flanks allow solder fillet to rise along the walls of the package and can be visually inspected using an inexpensive camera. Preceding leadless packages needed expensive X ray to enable such inspection. The centre pad has been enlarged to allow a via under pad. The pad-to-pad clearance has also been increased to enable routing to the centre pad on the top layer of the PCB. It features the same electrical specifications as the leaded alternative while offering significant space savings.

Nexperia's Sugested MicroPak (XSON5, SOT8065) packages

- Smallest leadless package that supports Automated Optical Inspection
- Breakthrough technology towards miniaturisation
- Includes families: HC(T), AHC, AUP, LVC, LVnT
- 1.1 mm x 0.85 mm x 0.47 mm
- Uses the same die as SOT353
- ~75% PCB area saving compared to SOT353
- Zero delamination, MSL 1
- Uniform 7 mm Sn layer on pad sides and bottom
- RoHS and dark green compliant



3. Recommended products

Product	Description	Key part numbers
Signal processing		
Inverters/Buffers/ Logic gates/Registers	AHC(T) product family, V_{cc} 2-6 V (4.5-5.5 V)	74AHC08BQ-Q100
	HC(T) product family, V_{cc} 2-6 V (4.5-5.5 V)	74HC2G08DC-Q100
	LVC product family, V_{cc} 1.2-3.6 V	74LVC126ABQ-Q100
	AUP product family, V_{cc} 0.8-3.6 V	74AUP2G80DC-Q100
	HCS product family, V_{cc} 2-6 V, true Schmitt trigger inputs	74HCS594BQ-Q100
	XSON5 – smallest leadless package with AOI	74AHC1G04GZ-Q100
Translators	LVC product family, V_{cc} 1.2-5.5 V	74LVC1T45GM-Q100
	AVC product family, V_{cc} 0.8-3.6 V	74AVC1T45GW-Q100
	NXU product family, fixed direction, dual supply	NXU0104GU12-Q100
	HC(T) product family, V_{cc} 2-6 V (4.5-5.5 V)	74HC1G66GW-Q100
	LSF product family, bi-directional translators with auto-direction sensing	LSF0101GW-Q100
	NXS product family, bi-directional translator with auto-direction sensing with signal acceleration on rising edge	NXS0506GU-Q100
	NXB product family, bi-directional translator with auto-direction sensing with signal acceleration on rising and falling edge	NXB0108BQ-Q100
Switches/Multiplexers	SP8T-Z and SP4T-Z analog switches	NMUX1308BQ-Q100
	Single-pole double-throw analog switches	XS5A1T4157-Q100
Resistor equipped transistors (RETs)	SOT23/SOT323/DFN1412D-3/DFN1110D-3/DFN1006B-3 50 V, 100 mA single NPN RETs, various resistors	PDTC143XQB-Q
	SOT23/SOT323/DFN1412D-3/DFN1110D-3/DFN1006B-3 50 V, 100 mA single PNP RETs, various resistors	PDTA144WMB

4. References

Nexperia handbooks

MOSFET and GaN FET application handbook

ESD Application Handbook

Bipolar Junction Transistor (BJT) Application Handbook

Diode fundamentals, characteristics and applications

Logic product features and application insights

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