

Paralleling of Nexperia GaN FETs

How to overcome challenges in Paralleling GaN FETs and increase the power capability of a Power design

Introduction

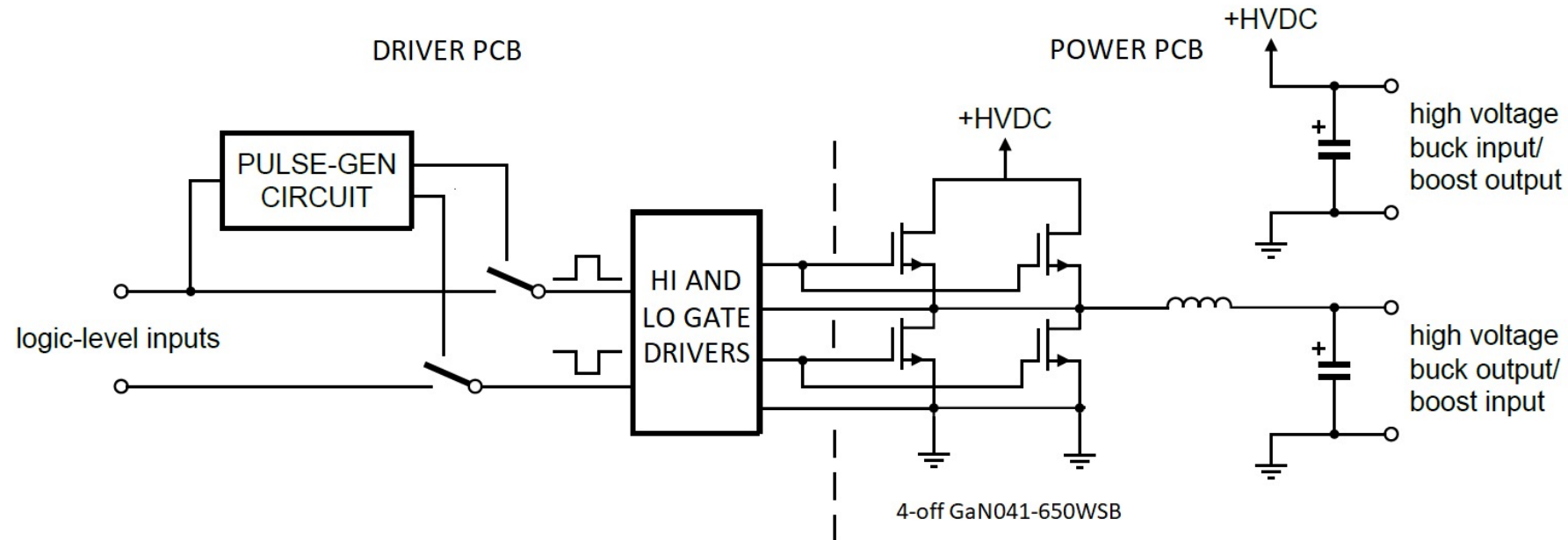
- Scott Durkin
- Senior GaN Applications Engineer

- Giuliano Cassataro
- GaN Marketing & Commercial Director



Half-bridge Functional Block Diagram

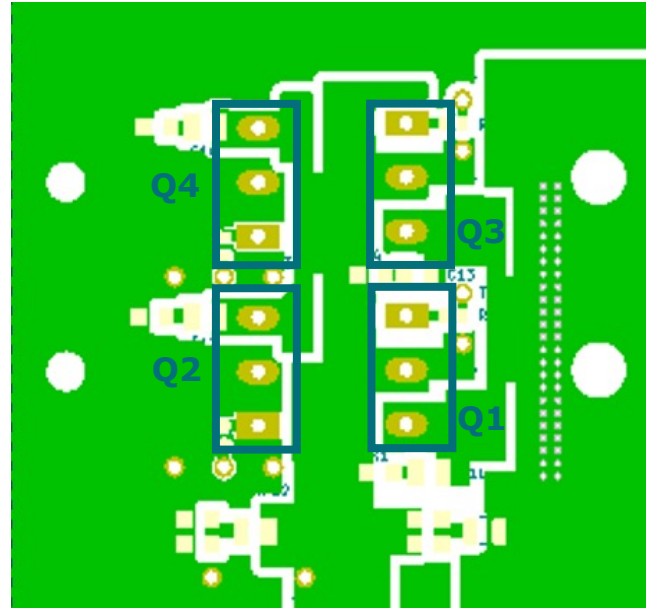
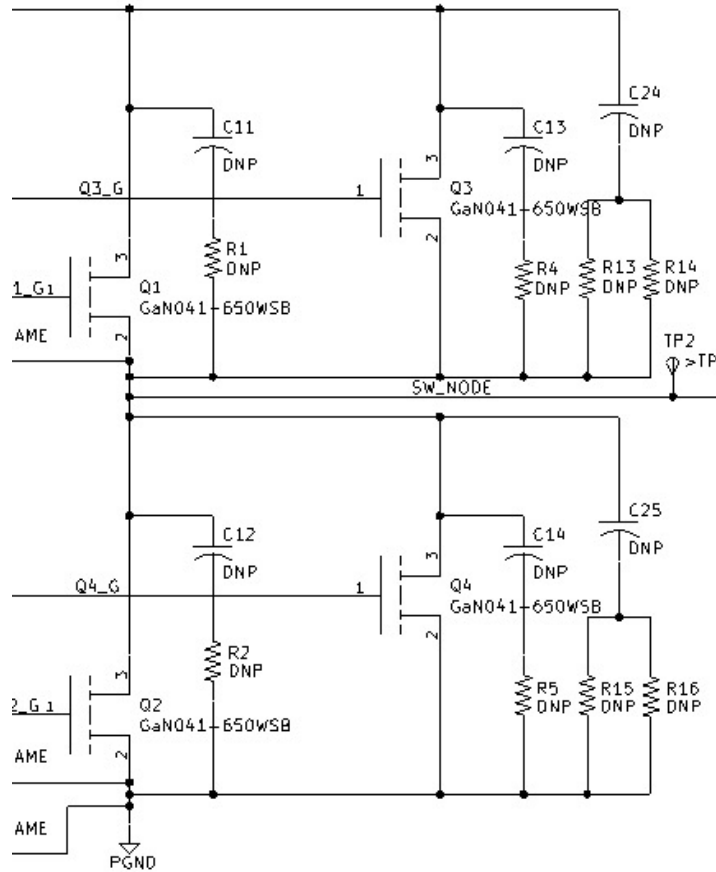
- The Functional Block Diagram of the Half-bridge is shown below.



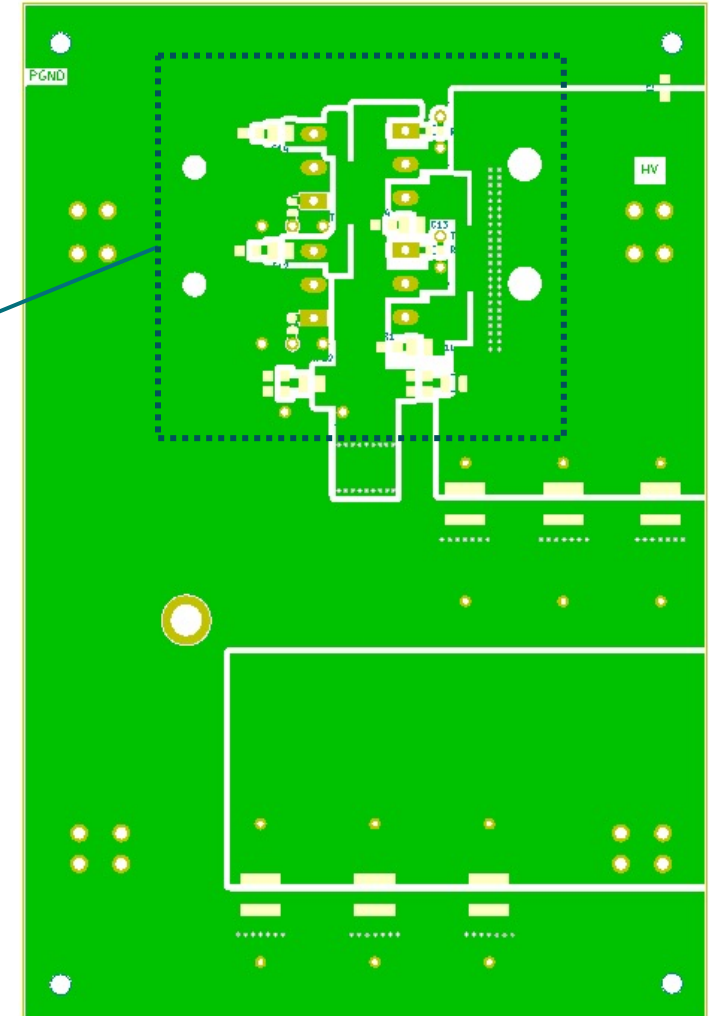
Recommendations for Paralleling Nexperia GaN FETs

- Symmetrical placement of components, tracking and Gate-Source loops is KEY so that the effective impedance paths are as matched as much as possible.

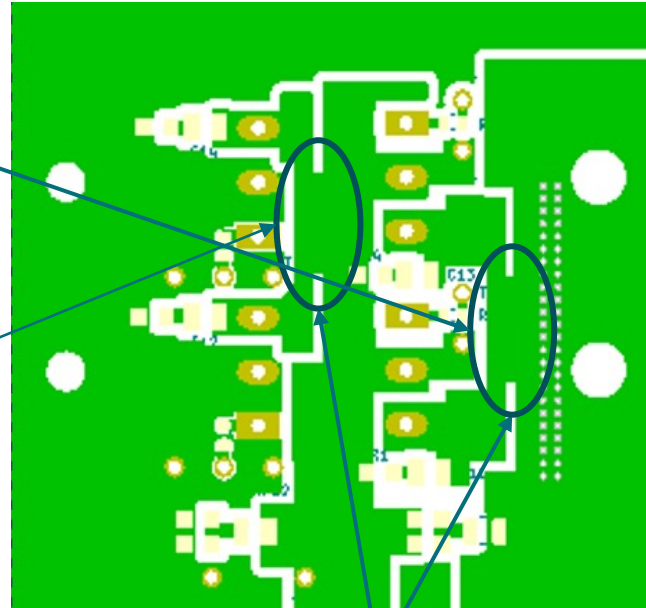
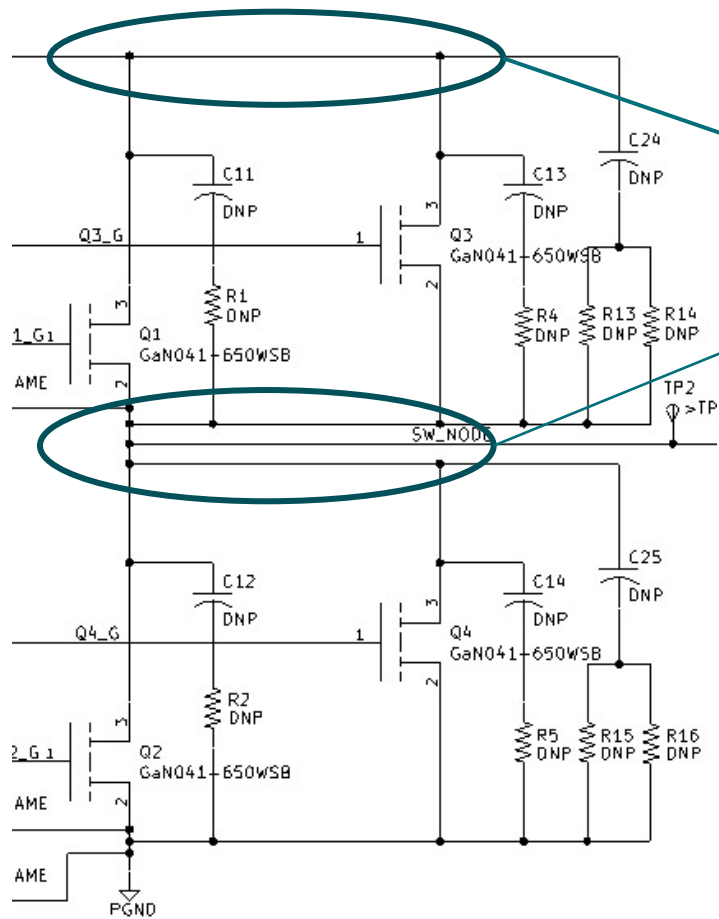
Recommendations for Paralleling Nexperia GaN FETs



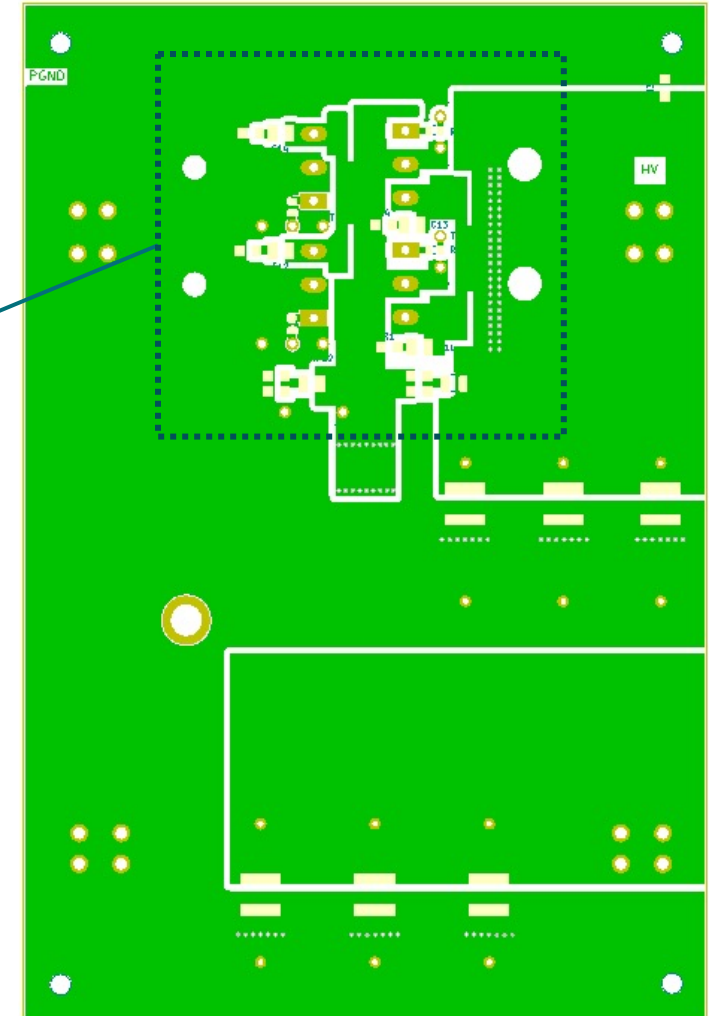
Placement of the four TO-247 GaN FETs



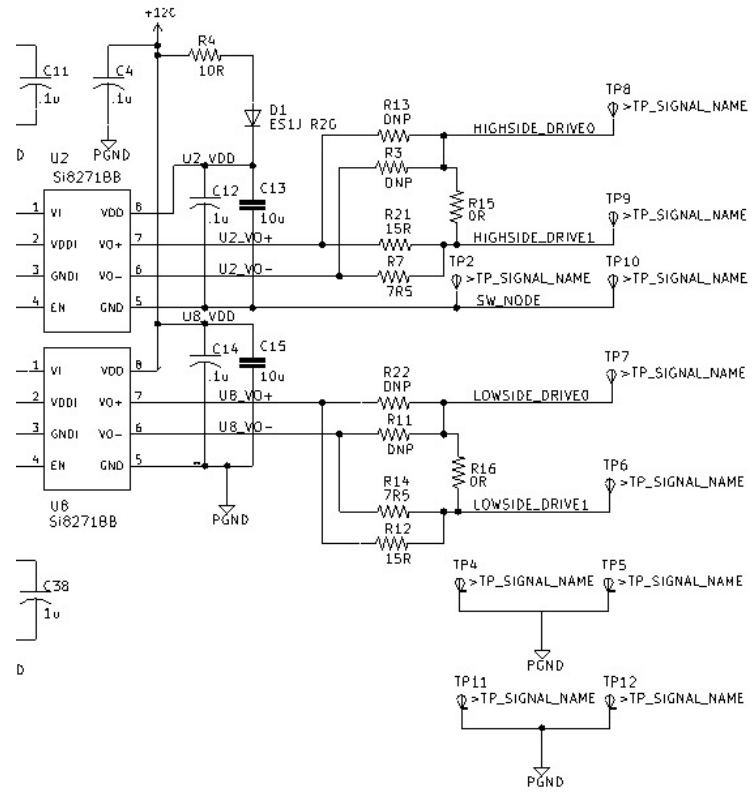
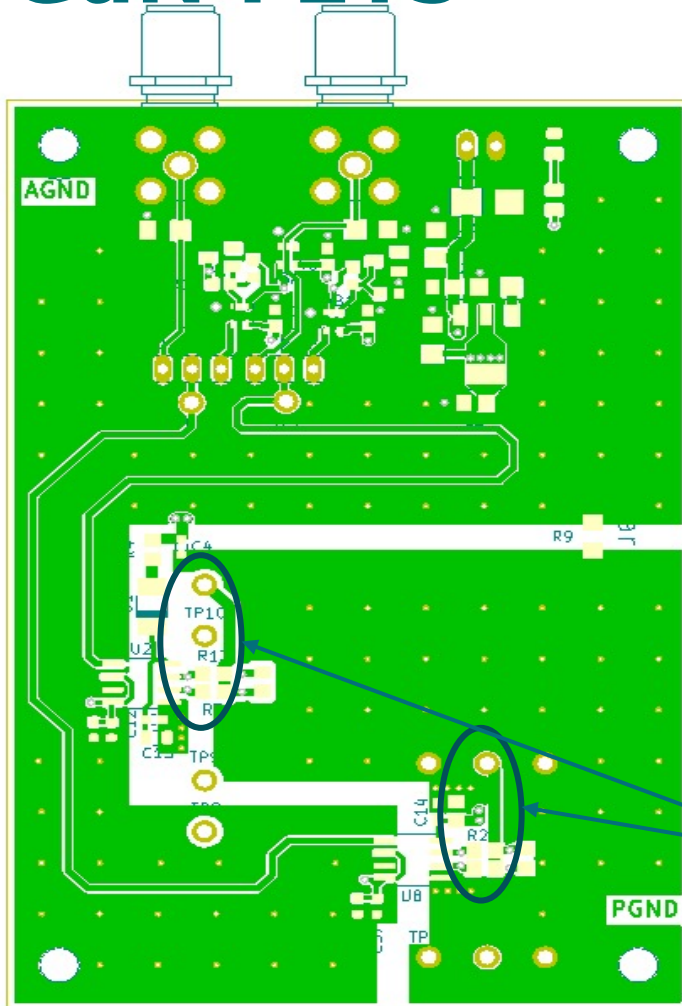
Recommendations for Paralleling Nexperia GaN FETs



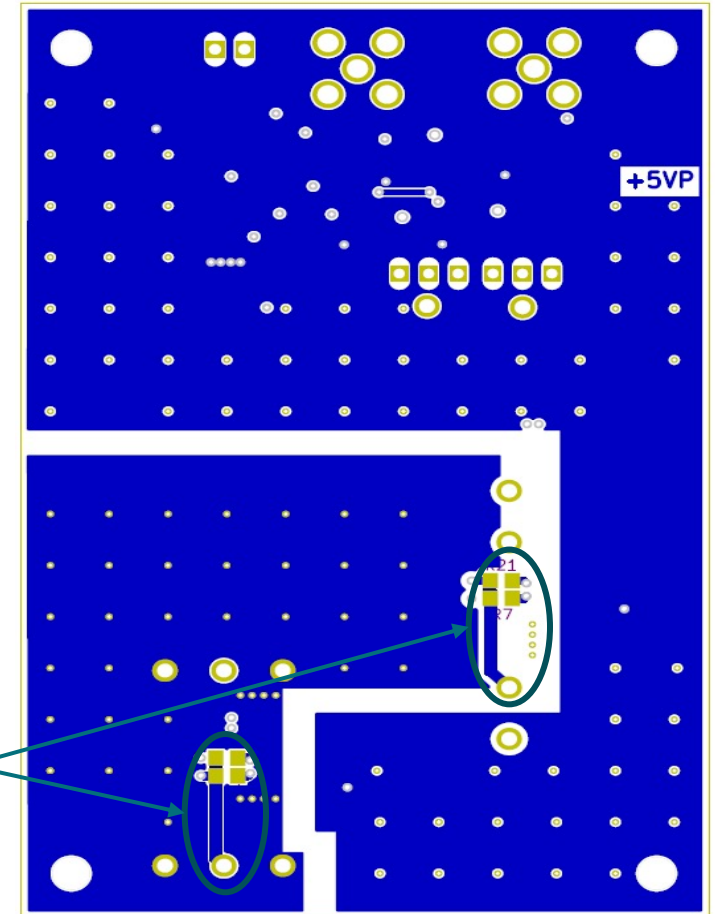
Drain connections have been made symmetrically to switch node and HV.



Recommendations for Paralleling Nexperia GaN FETs

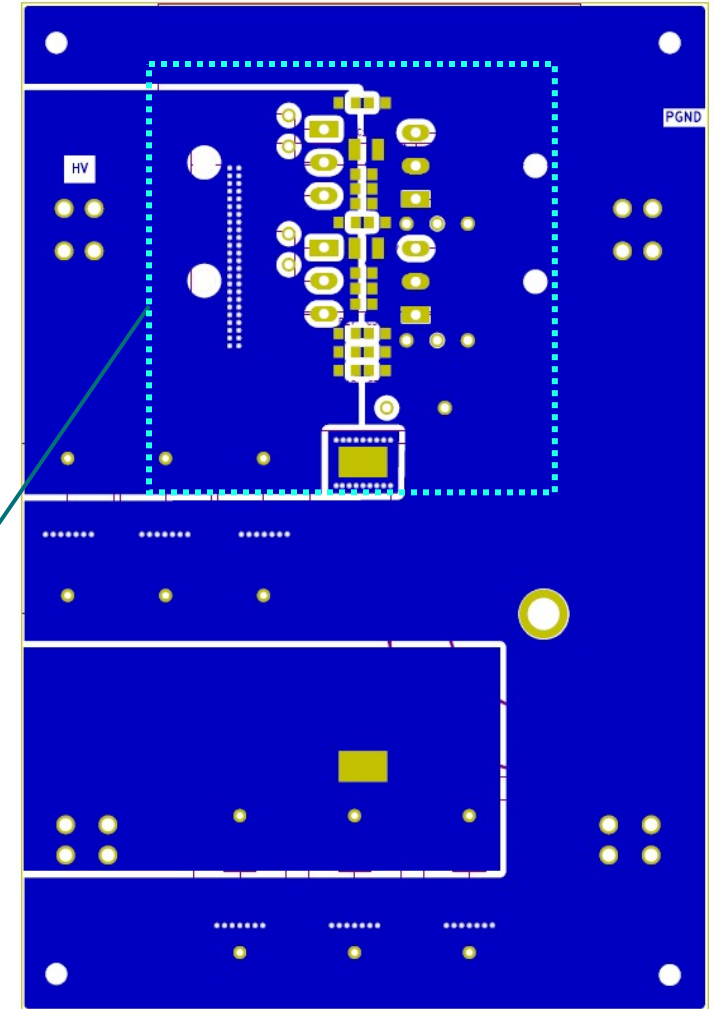
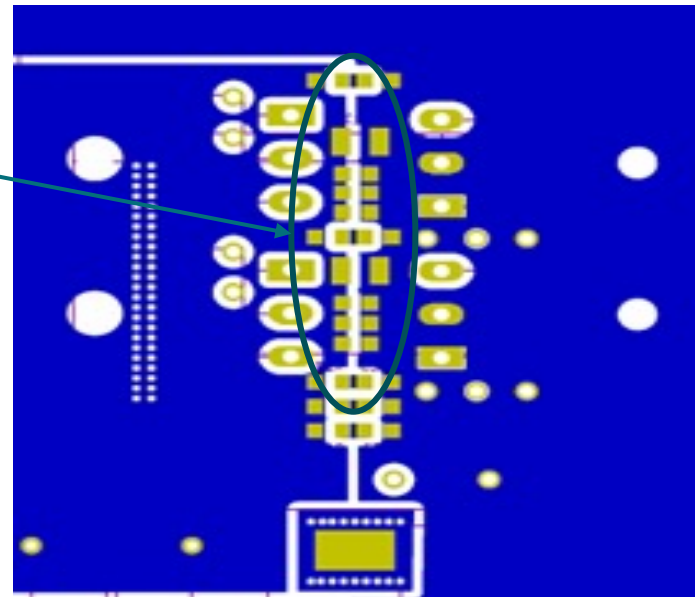
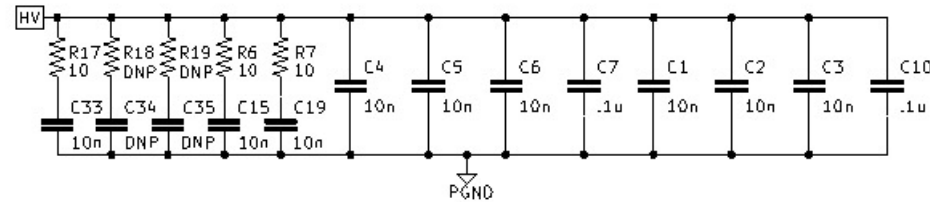


Symmetrical gate drive connections

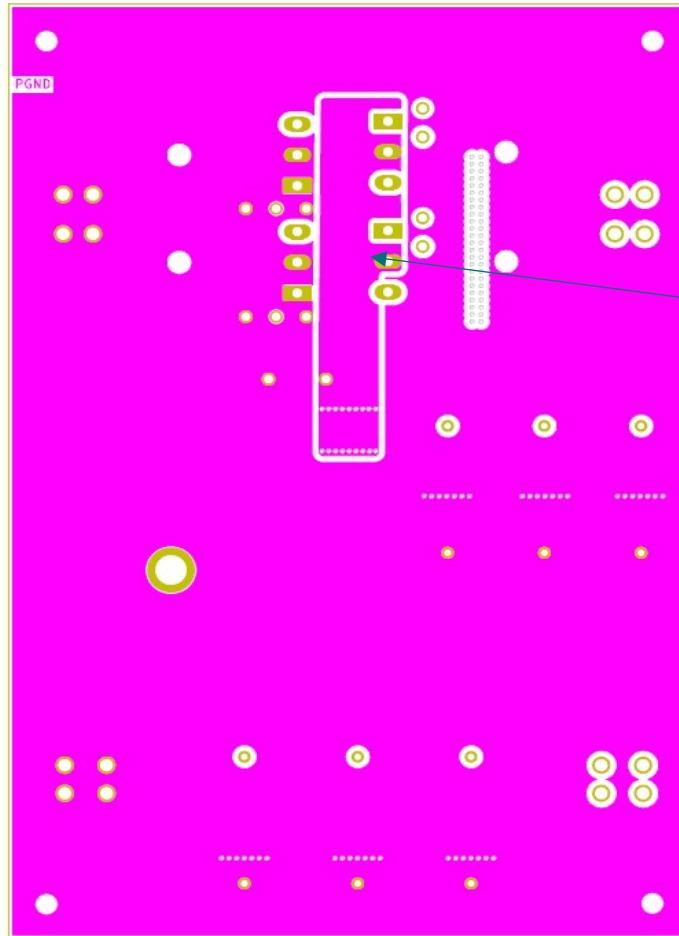


Recommendations for Paralleling Nexperia GaN FETs

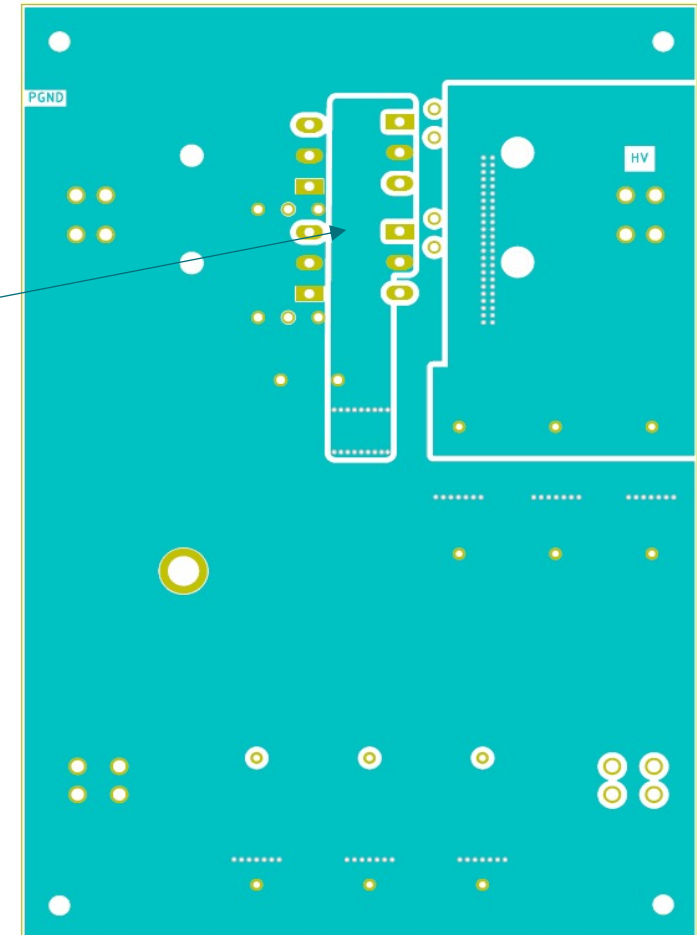
RC snubbers are required to damp any resonance on the DC bus, and along with local decoupling are placed as close as possible to each GaN FET.



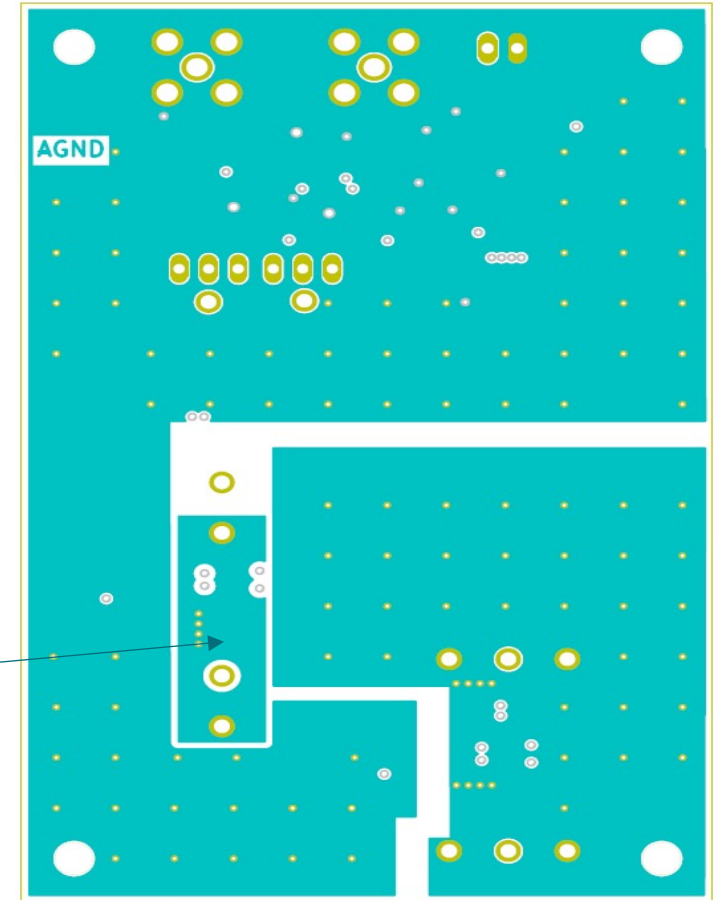
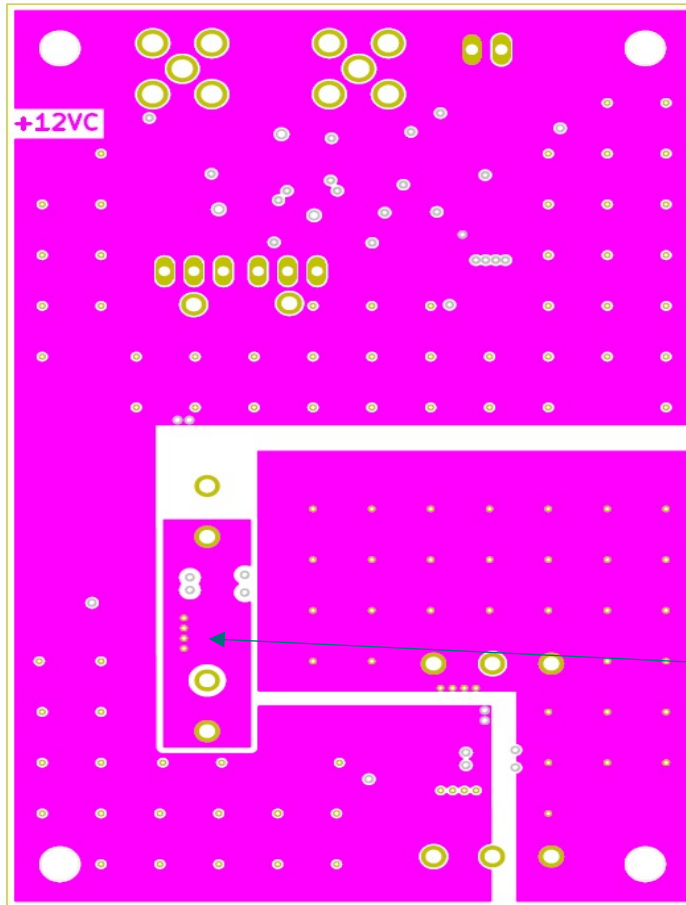
Recommendations for Paralleling Nexperia GaN FETs



Switch node should be as compact as possible.

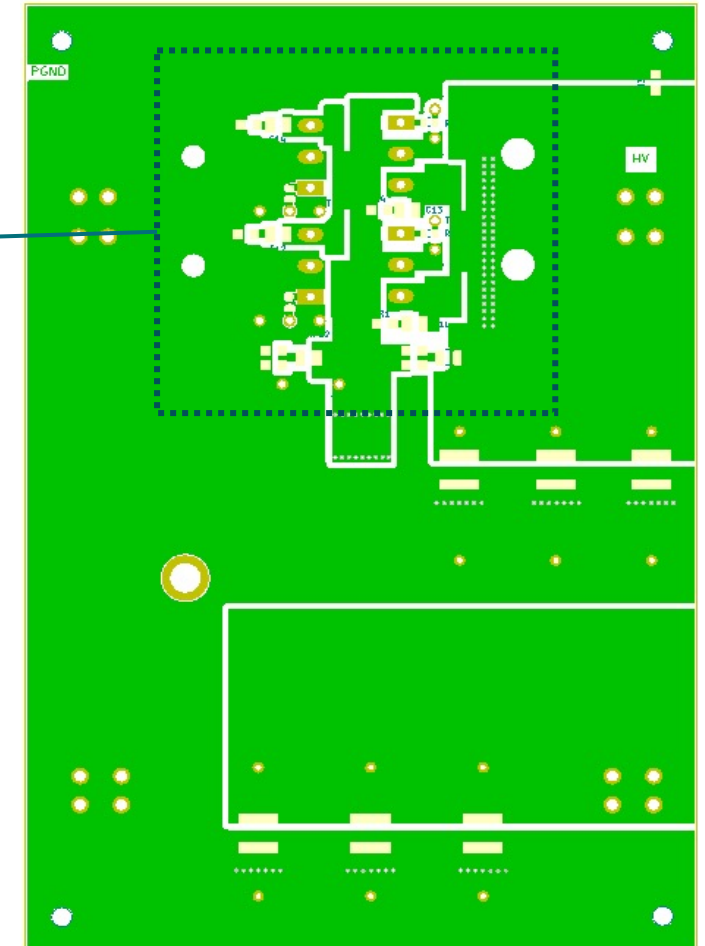
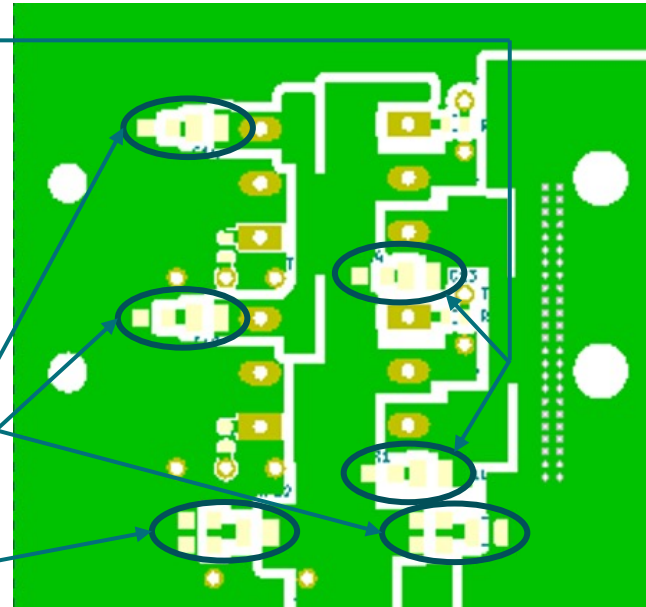
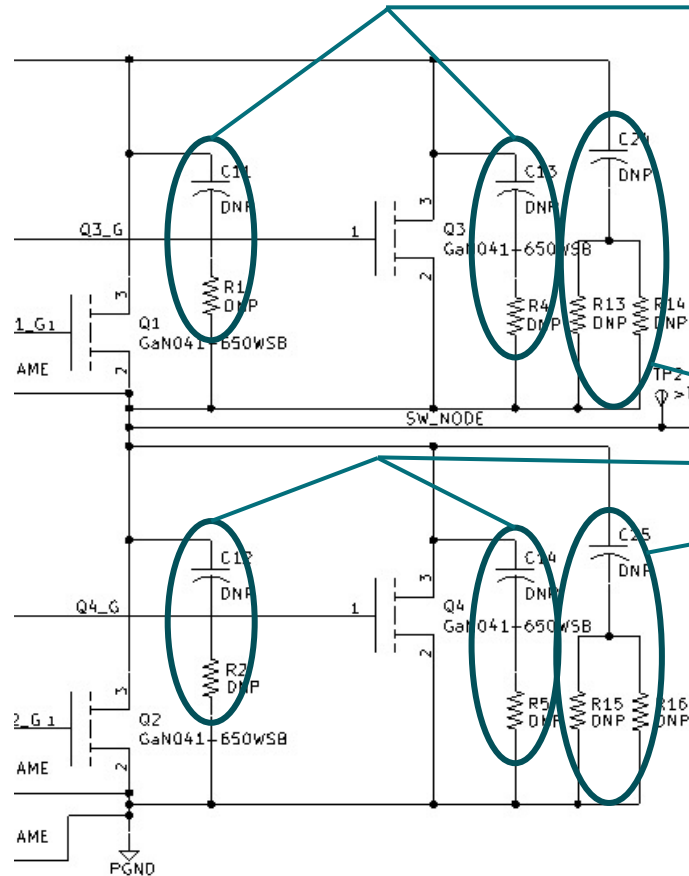


Recommendations for Paralleling Nexperia GaN FETs



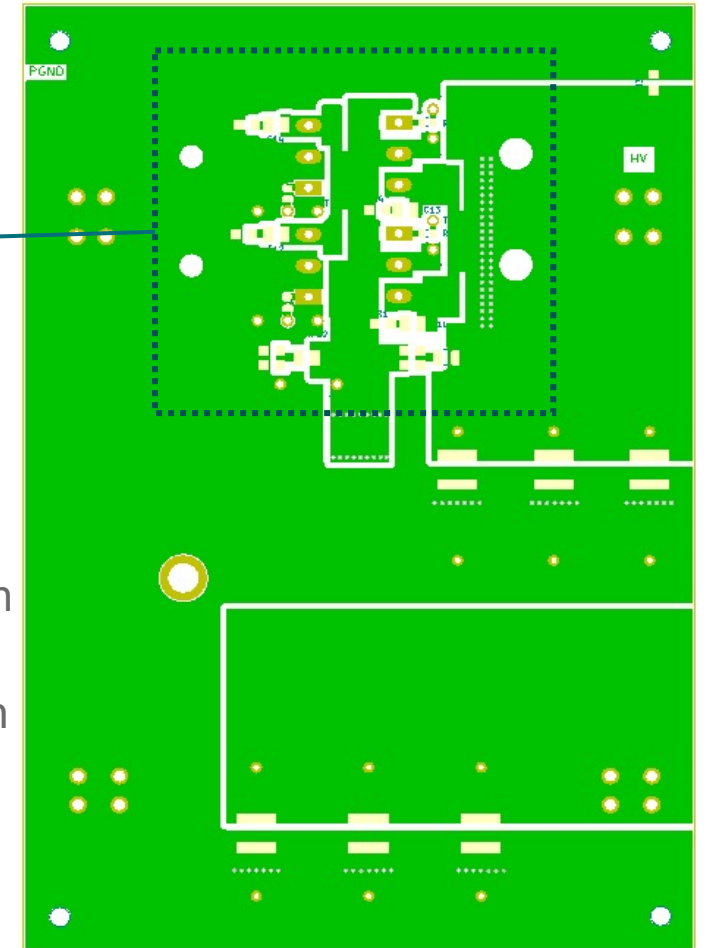
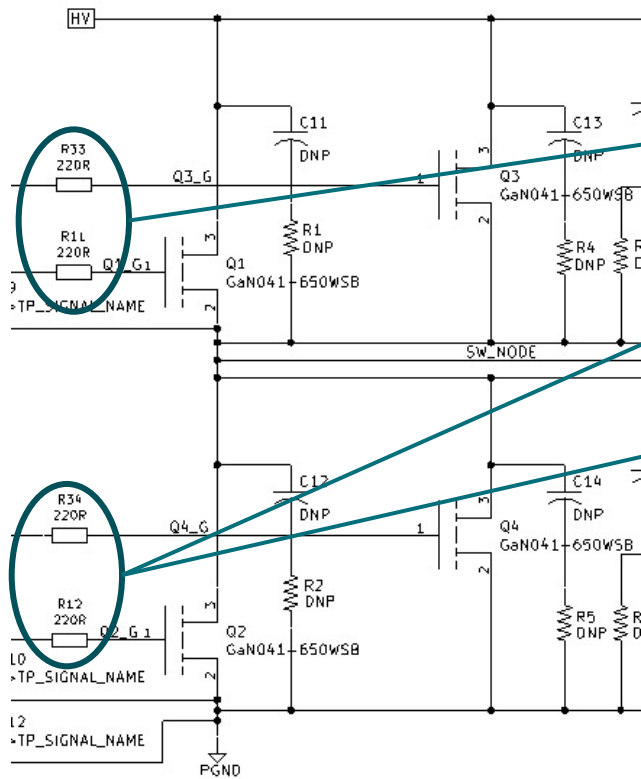
Switch node should be as compact as possible.

Recommendations for Paralleling Nexperia GaN FETs



Provision should be made in the design for Switch node snubbers. However, these may not actually need to be populated.

Recommendations for Paralleling Nexperia GaN FETs



Each GaN FET must have a Ferrite bead in the Gate circuit. The recommended component to be used in conjunction with GaN041-650WSB devices is BLM18AG221SN1D, which has a typical impedance of 220 ohms at 100 MHz.

Recommendations for Paralleling Nexperia GaN FETs

- Drivers should be physically close to the GaN FET.
- If they are located on a separate PCB due to design, placement or packaging constraints, then short wide tracks or ideally multiple planes, in association with large gauge terminals soldered between the boards, is advised.
- Use of non-soldered connectors, such as plug and sockets are not recommended in the Gate-Source loop as they typically increase the inductance, leading to an increased risk of oscillation.

Recommendations for Paralleling Nexperia GaN FETs

- Paralleled GaN FETs should be thermally very well connected to each other so that the temperatures are equalised as much as possible, leading to distribution of current equally.

Single-Shot Staircase test to 114 A at 400 V Bus, 100 kHz



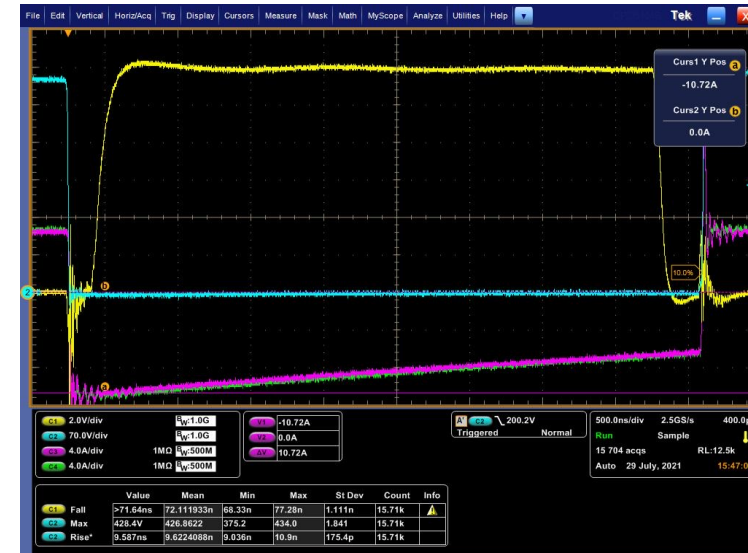
- Yellow and Blue Traces – Lowside GaN FET Gate signals, Magenta Trace – Inductor current, Green Trace – Switch Node voltage

Single-Shot Staircase test to 114 A at 400 V Bus, 100 kHz



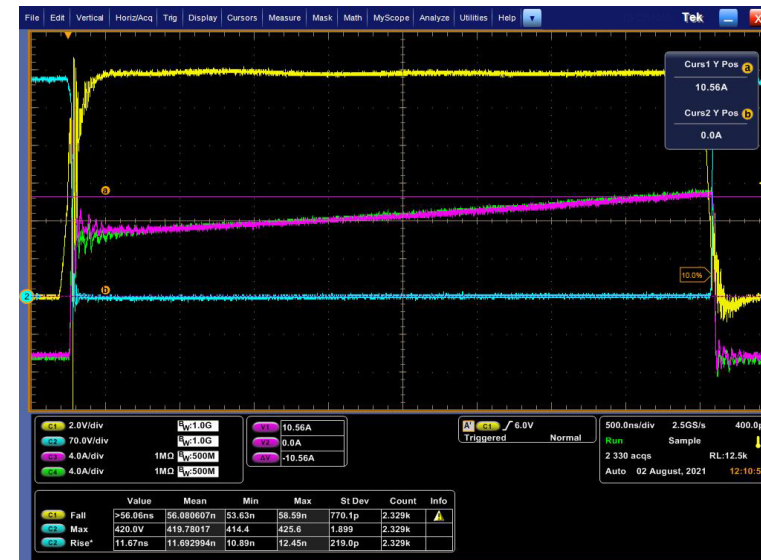
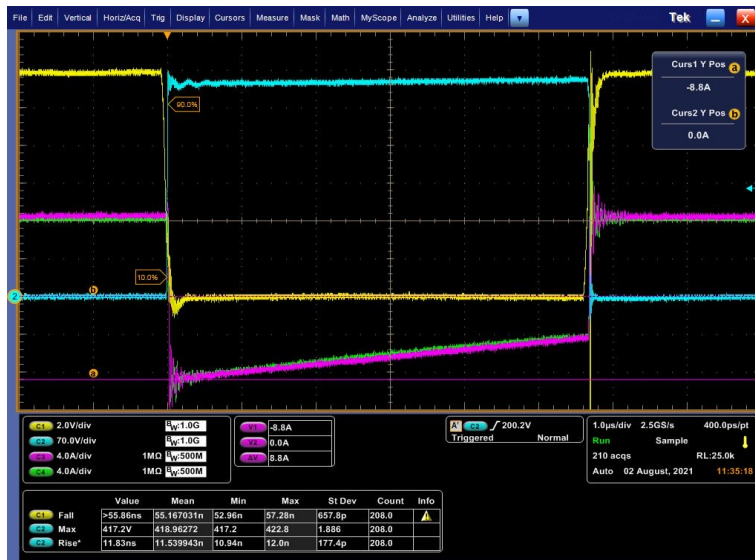
- Yellow Trace – Lowside GaN FET Gate signal as trigger, blue trace – Switch node Voltage, magenta and green traces – Lowside GaN FET Device current.
- Note magenta and green are the measured GaN FET currents, showing excellent current sharing between devices.

Buck Mode : 400 V Input, 225 V Output, 6.6 kW, 100 kHz



- Yellow Trace – Lowside GaN FET gate signal as trigger, blue trace – Switch node Voltage, magenta and green traces – Highside (left) or Lowside (right) GaN FET device currents.
- Note magenta and green are the measured GaN FET currents, showing excellent current sharing between devices.

Boost Mode : 225 V Input, 400 V Output, 6.6 kW, 100 kHz



- Yellow Trace – Lowside GaN FET gate signal as trigger, blue trace – switch node Voltage, magenta and green Traces – Highside (left) or Lowside (right) GaN FET device currents.
- Note magenta and green are the measured GaN FET currents, showing excellent current sharing between devices.

Further information

Please visit [Nexperia.com/GaN-FETs](https://www.nexperia.com/GaN-FETs)

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Whether designing a motor drive/controller for the next generation of battery-electric vehicles, or a power supply for the latest 5G telecommunication networks, Nexperia's GaN FETs will be key to your solution. Offering high power performance and high-frequency switching, the design and structure of our normally-off GaN FET products ensure standard, low-cost gate drivers can be used in your design.

Featured product	Description
GAN063-650WSA	650 V, 50 mΩ Gallium Nitride (GaN) FET in a TO-247 package
GAN041-650WSB	650 V, 35 mΩ Gallium Nitride (GaN) FET in a TO-247 package
GAN039-650NBB	650 V, 33 mΩ Gallium Nitride (GaN) FET in a CCPAK1212 package
GAN039-650NTB	650 V, 33 mΩ Gallium Nitride (GaN) FET in a CCPAK1212I package



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Nexperia GaN FETs - Performance, efficiency, reliability brochure



MOSFET and GaN FET Application Handbook



Focus package: CCPAK

Application notes & white papers



Understanding Power GaN FET data sheet parameters
AN90005



Circuit Design and PCB Layout Recommendations for GaN FET Half Bridges
AN90006



GaN FET technology and the robustness needed for AEC-Q101 qualification
White paper

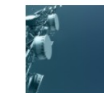
Latest news and blogs



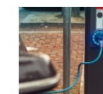
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GaN FETs help push 80 PLUS Titanium grade



Apr 22, 2021
GaN shines a light on PV inverter efficiency



Feb 1, 2021
Eliminating EMC By Replacing A MOSFET With A GaN ...



Oct 12, 2020
CCPAK - the option of top-side cooling for GaN FETs



Sep 30, 2020
GaN FETs: Why cascode?



Aug 18, 2020
Power GaN FETs: a strategic approach to bring the ...



Quick Learning: Cascode Vs E-Mode – which to use in your ...



Quick Learning: What is CCPAK? (Surface-mount packaging for ...



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questions and insights

EFFICIENCY WINS.